



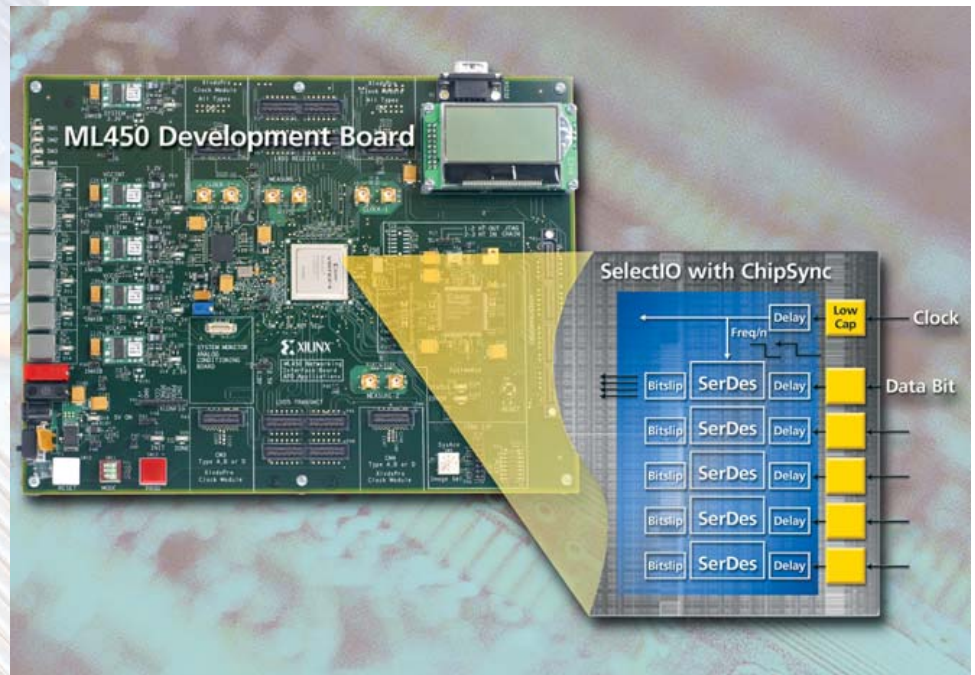
Virtex-4™ FPGA Source-Synchronous Interfaces Tool Kit

Powered by ML450 Platform

Today's telecom and networking systems use high-bandwidth interfaces based on LVDS and other differential I/O standards. These standards – and associated protocols such as SPI-4.2, SFI, RapidIO and HyperTransport – simplify system design by improving performance and signal integrity. However, they also pose a host of challenges for the system designer in ensuring device interoperability and standard compliance.

Virtex-4™ FPGAs help solve these challenges with more than 1 Gbps SelectIO™ parallel I/O featuring specialized ChipSync™ source-synchronous circuits. Designers can use most SelectIO as differential I/O without bank restrictions. Plus, Xilinx provides Virtex-4 FPGA development boards, as well as standards-compliant IP cores for major system interface protocols. This allows the designer to focus on the user application rather than interoperability and standards compliance.

With Virtex-4 FPGA Source-Synchronous Interface Tool Kit, designing networking, telecom, servers, and computing systems is faster and easier than ever before.



Faster, Easier Source-Synchronous Interfaces Implementation

Design with major differential I/O standards in networking, computing standards

- Single Data Rate (SDR) and Double Data Rate (DDR) differential interfaces
- OIF SPI-4.2 (POS-PHY level 4), SFI-4 and XSBI interfaces
- HyperTransport and RapidIO interfaces

Finish faster using pre-engineered IP cores and reference designs

- IP cores for SPI-4.2 and RapidIO
- Reference designs for SFI-4, DDR 1 SDRAM controller

Realize Over 1 Gbps performance with the unique built-in ChipSync technology

- ChipSync source-synchronous technology embedded in every I/O
- Dynamic programmable delay/data centering with per-bit de-skew on every I/O
- Bitslip module for training patterns
- Internal SerDes modules and regional clocks

Discover the complete hardware development and evaluation platform

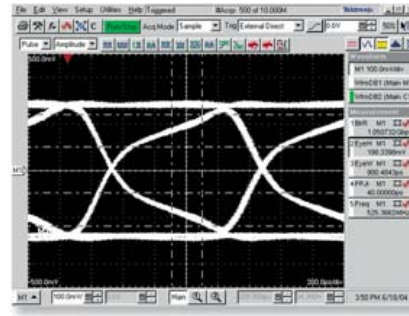
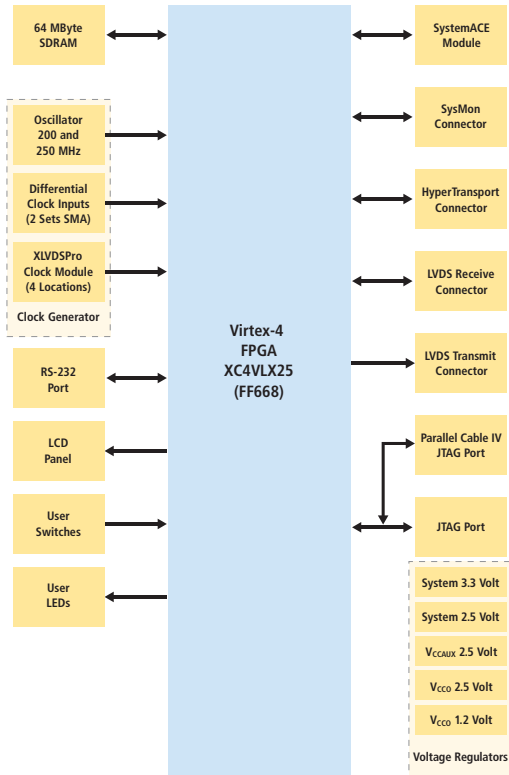
- Based on 4VLX25
- Support for eight clock sources; differential clock inputs
- Connectors for multiple system interface standards
- On-board memory and LCD display

Hardware Platform Details

Use these platforms to develop and evaluate multiple source – synchronous interfaces of over 1 Gbps operation with Virtex-4 FPGAs, IP, and reference designs.

System Interface Support: Design with SPI-4.2, SDR SFI-4, SDR XSBI, HyperTransport, and RapidIO interfaces. Proprietary interfaces based on LVDS can also be developed.

ML450 Hardware Development Platform Block Diagram



Example: Tx Diagram. 1 Gbps, 2.5V LVDS, PRBS23 pattern.

ML450 Specifications

- FPGA
 - Up to 24,192 logic cells
 - Up to 1.3 Mb block RAM
 - Up to 448 user I/O; 224 differential pairs
 - Built-in ChipSync source-synchronous technology
 - 48 XtremeDSP™ slices
 - 8 DCMs
- 64 MB DDR 1 SDRAM
- LVDS, HyperTransport, RS232 connectors
- 64x128 pixel graphics LCD
- 8 clock sources

Complete Solution: The kit comes with the following Xilinx Productivity Advantage (XPA) options:

- ML450 Platform including Compact Flash, clock modules, documentation, reference designs, cables, and evaluation software
- ISE Foundation Software
- IP Cores: SPI-4.2, RapidIO*, and GFP*
- Training, Premium, and Titanium services

* Check with your Xilinx sales representative for availability

Take the Next Step

Buy the Source-Synchronous Interfaces Tool Kit today and get started on your design. For more information about the kit, the Virtex-4 FPGA family, ChipSync technology, and available optional IP, visit www.xilinx.com/virtex4

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