High-Performance Memory Interfaces Made Easy

Xilinx 90nm Design Seminar Series:

Part IV

Xilinx - #1 in 90 nm

We Asked Our Customers:

What are your challenges?

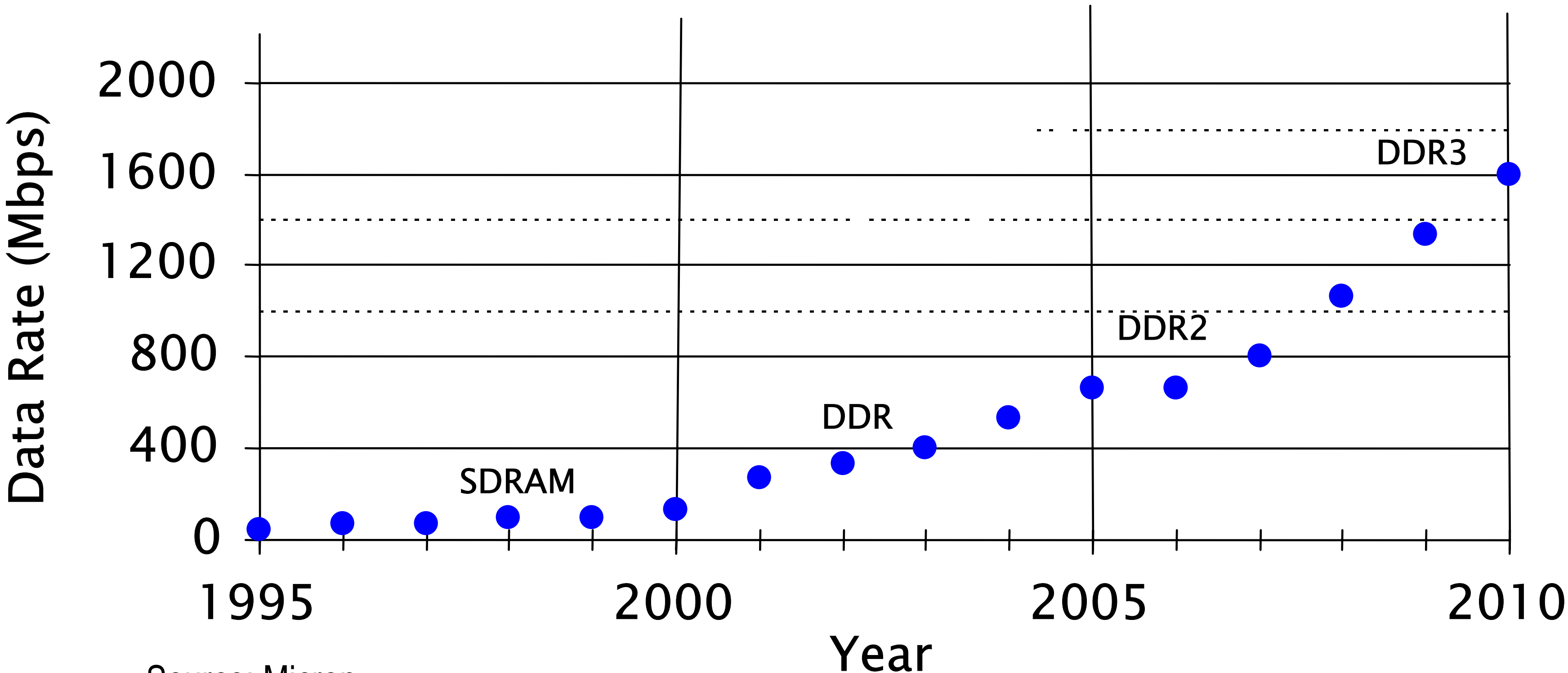
- Shorter design time, faster obsolescence
- More competition, increasing cost pressure
- Demanding complexity and performance
- Power consumption and thermal issues
- Signal integrity problems caused by faster I/O
- Interfacing to high-performance memories

- Today's seminar addresses ***Memory Interfaces***

Agenda

- Memory Trends
- Design Challenges and Solutions
- DDR2 SDRAM Interface
- Summary

Mainstream Memory Data Rates

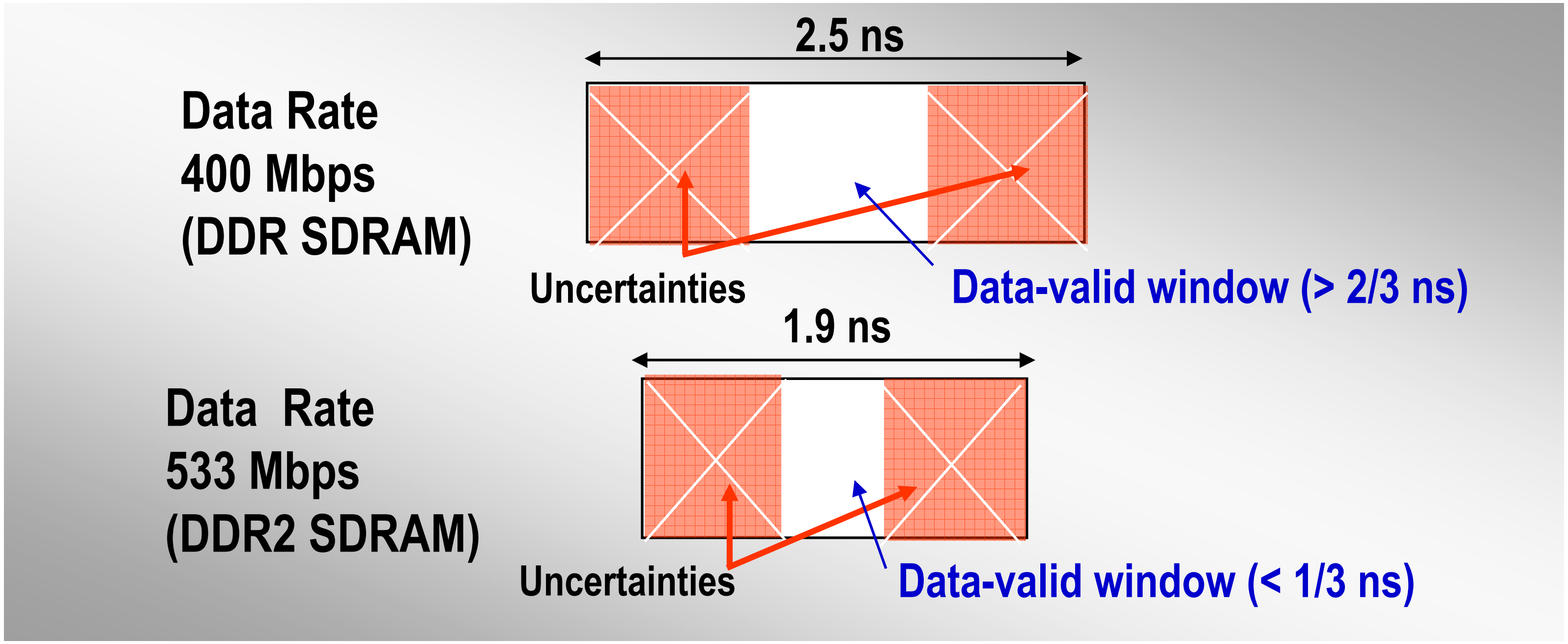


Source: Micron

Mainstream memory data rates doubling every four years

Shrinking Timing Margins

- Data-valid window shrinks faster than clock period
  - Faster data rates but similar device and system uncertainties



Interface timing becomes more demanding

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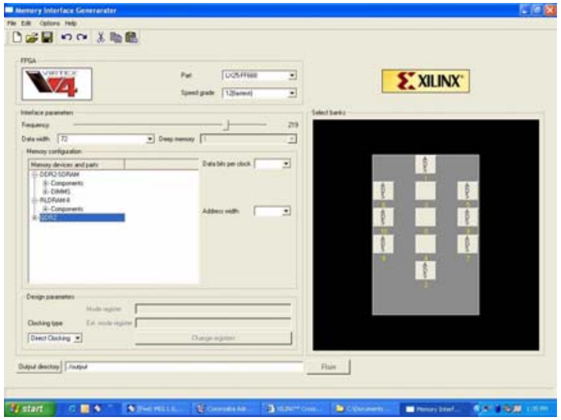
Memory Interface Design Can be Challenging

1. Timing-critical physical layer
   – Read-data capture
   – Meeting the timing budget with reliable design margins
2. High bandwidth system requirements
   – Data Rate x Bus Width
   – Resolving signal integrity issues
   – Meeting I/O placements and board routing requirements
3. Complex memory controller design

Based on more than 300 customer surveys

Xilinx Makes it Easy

- Virtex-4 FPGA built-in silicon features
  - Chipsync™ in every I/O
- Hardware-verified designs for highest performance interfaces
  - DDR2 SDRAM, DDR SDRAM, QDR II SRAM, RLDRAM II
- Memory Interface Generator (MIG)
  - Generates your custom memory controller and physical layer interface in minutes using hardware verified designs



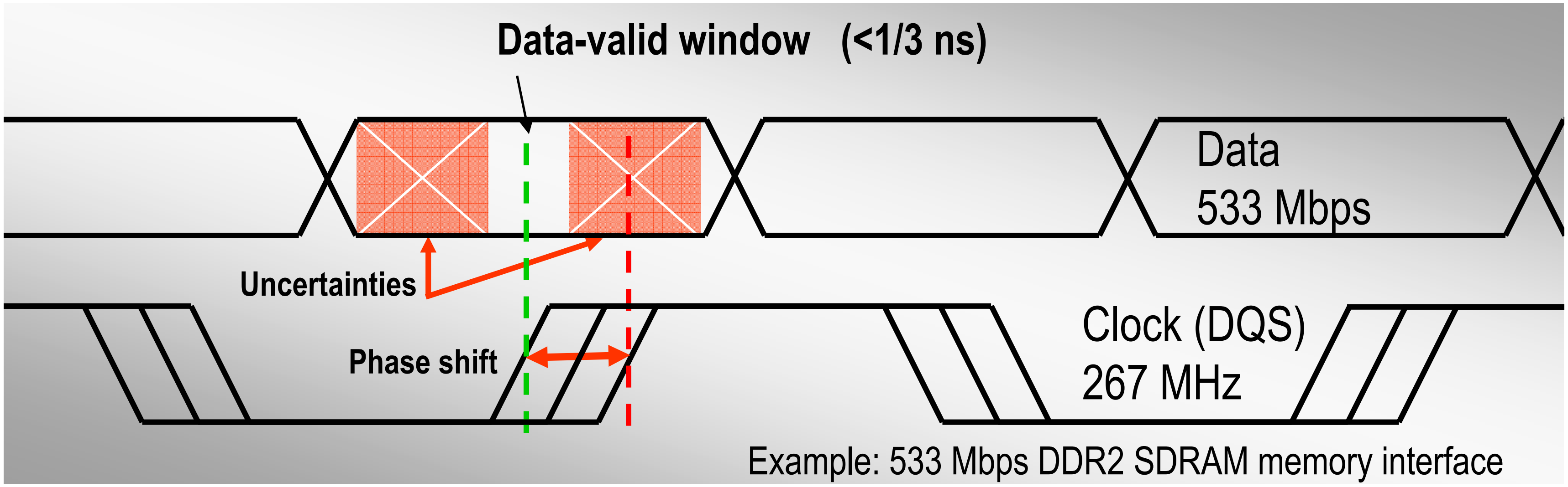
Memory Interface Generator

ML461- Development System

Timing-critical Physical Layer

Toughest Design Challenges

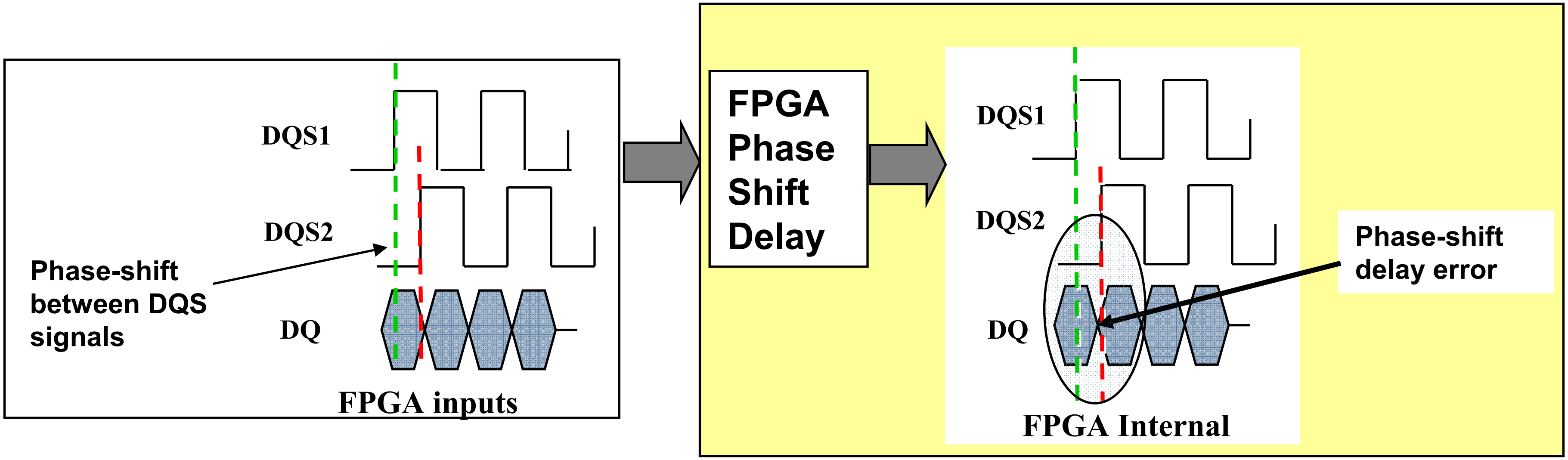
- Centering the clock to the data-valid window for read cycles
  - System conditions change the clock-to-data phase shift



Centering the clock to a shrinking data-valid window

Fixed Phase-Shift Delay Method

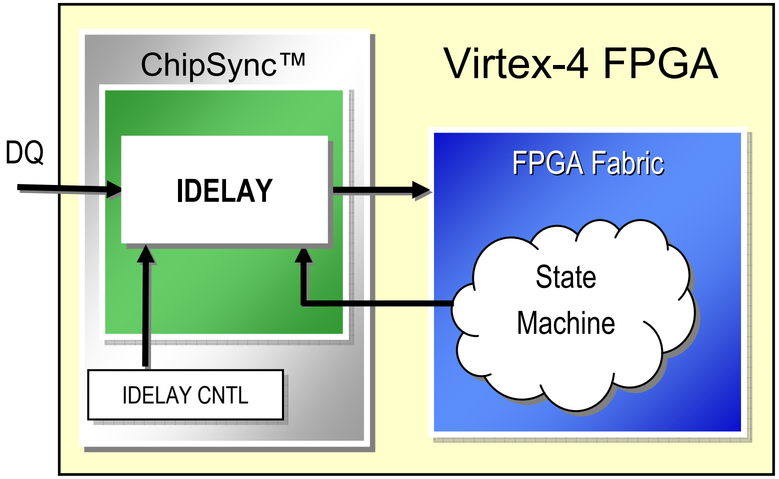
- Phase-shift determined at design time not at “run time”
  - In-system testing required for verification
- Phase-shift does not adjust for system variations
  - Delays between different clock (DQS) signals
    - Process, voltage, temperature

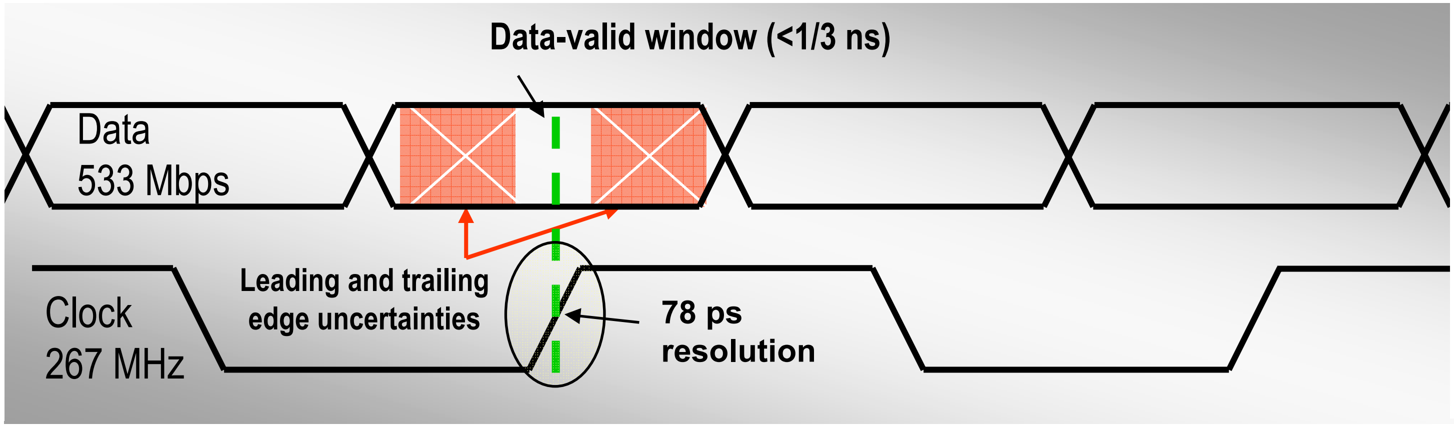


Fixed phase-shift delay erodes design margins

Precise Data-to-Clock Centering

- **Unique Virtex-4 FPGA solution with ChipSync IDELAY**
  - "Run time" centering of data-to-clock
  - 64 tap delays with 78 ps resolution
  - Maximizing design margins for higher system reliability





Not available in any other FPGA, ASIC or ASSP

High Bandwidth System Requirements

- Maximizing bandwidth : Data Rate x Bus Width
- Resolving signal integrity issues
- Meeting I/O placement and board routing requirements

Data Rate x Bus Width

- Any I/O can be used for Data, Strobe/Clock or Address/Controls
  - Chipsync built in every I/O
  - Any Data to Strobe ratio from x4 to x36 is supported
- Data rates of 600 Mbps for single-ended I/O standards
- Up to 259 Gbps data bandwidth using 432 Data bits
  - Superior SSO performance with innovative package design

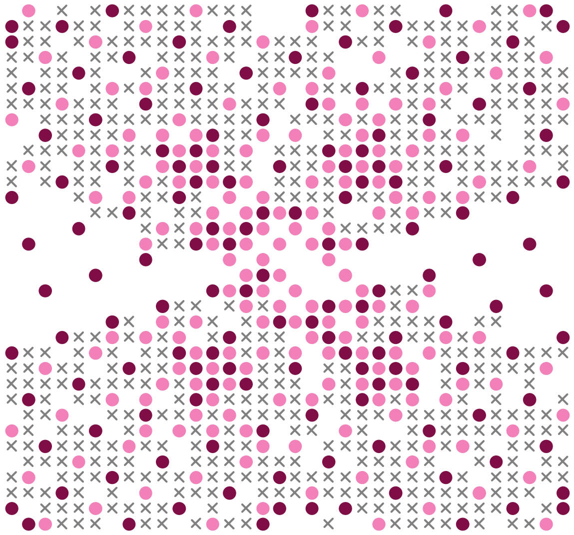
Virtex-4 Device	Pkg	Max Data width
LX25, LX40, LX60	FF668	144
LX40, LX60	FF1148	288
LX80, LX100, LX160	FF1148	360
LX100, LX160, LX200	FF1513	432

3 x higher bandwidth than competing solutions

Achieving Superior SSO Performance

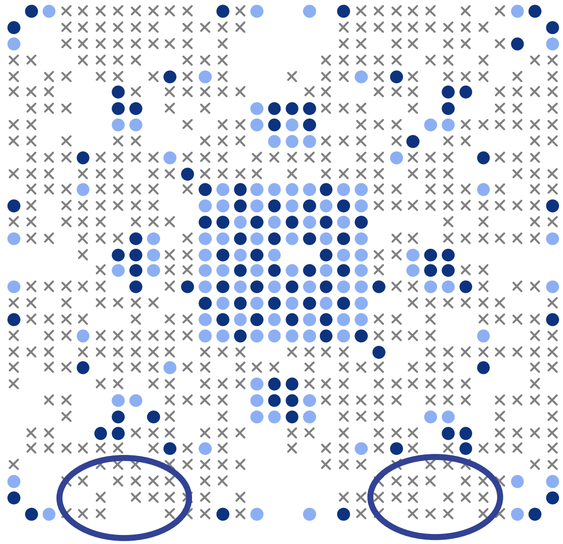
- Column-based architecture and SparseChevron™ package
  - Better power and ground distribution

Virtex-4 FF1148



Returns spread evenly

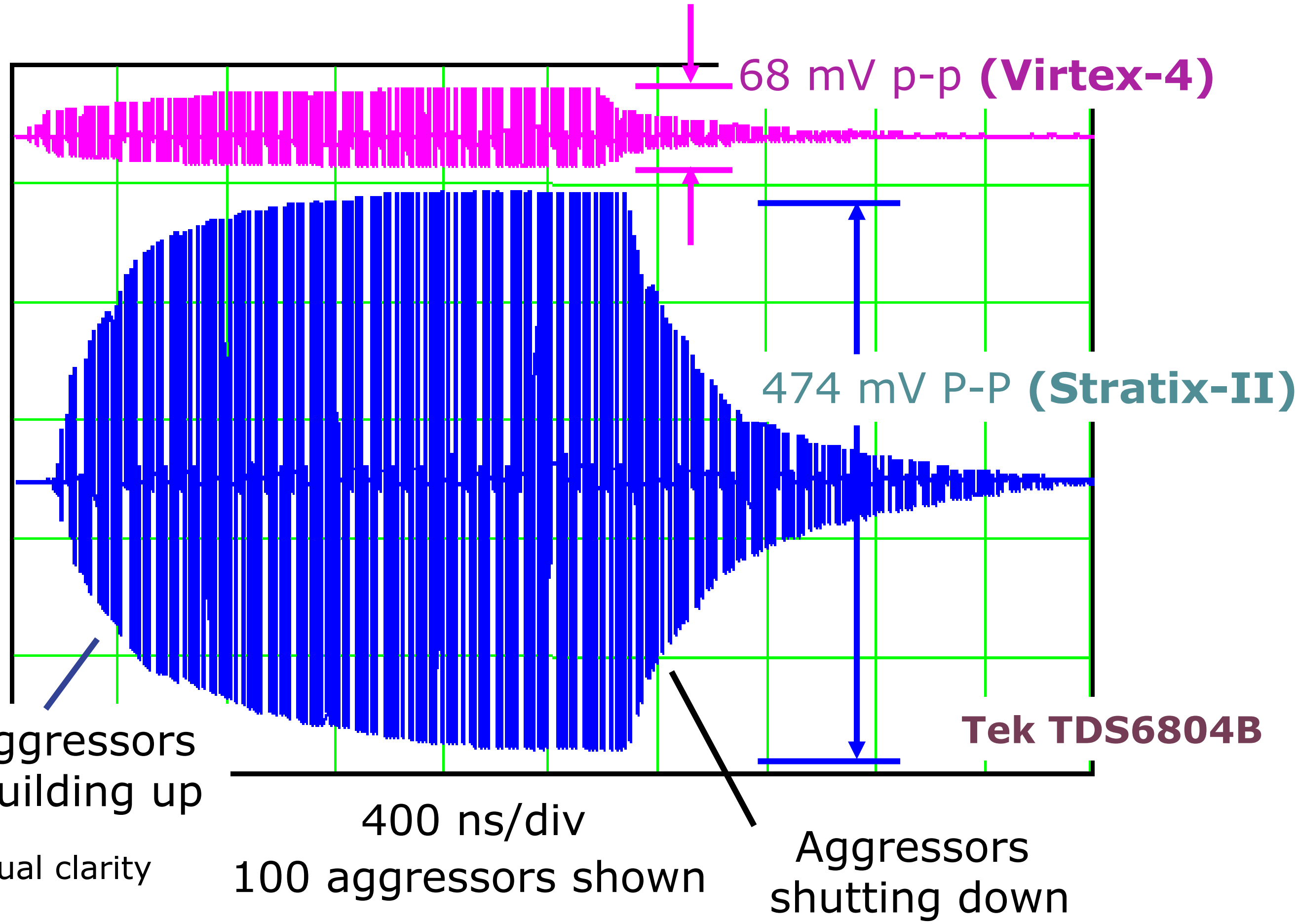
Stratix II F1020



Many regions devoid of returns

Better SSO performance than competing solutions

Accumulating Test Comparison



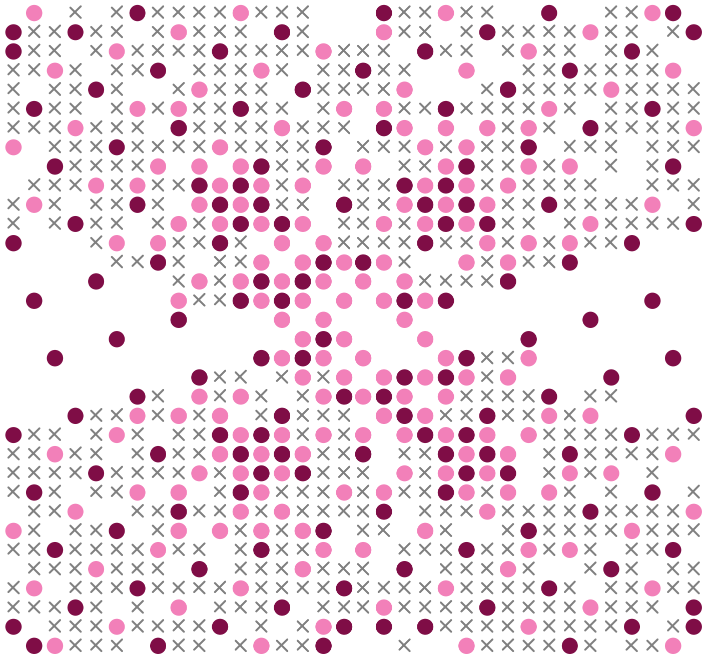
Waveforms offset for visual clarity

Source: Dr. Howard Johnson

7 x less crosstalk than competing solutions

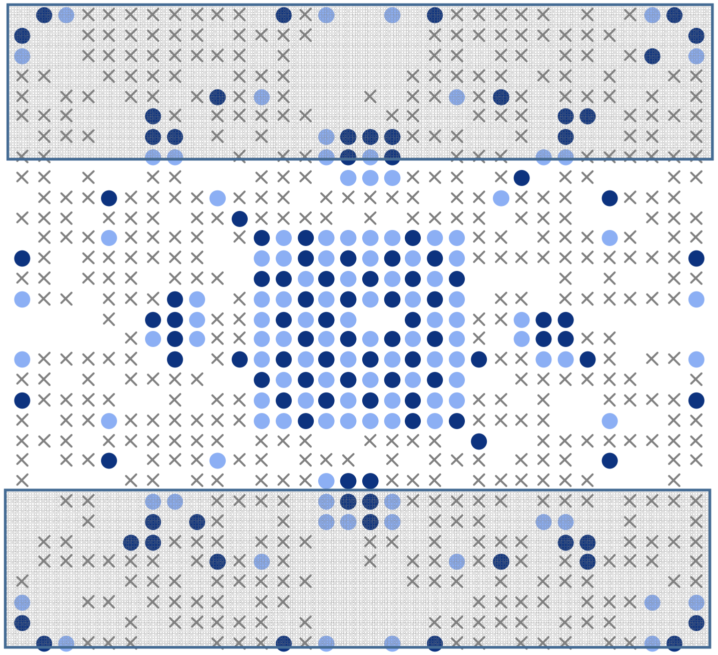
Meeting I/O Placement Requirements

Virtex-4 FF1148



Unrestricted I/O placements

Stratix II F1020



Memory I/Os restricted to top and bottom

3 x more data I/Os than competing solutions

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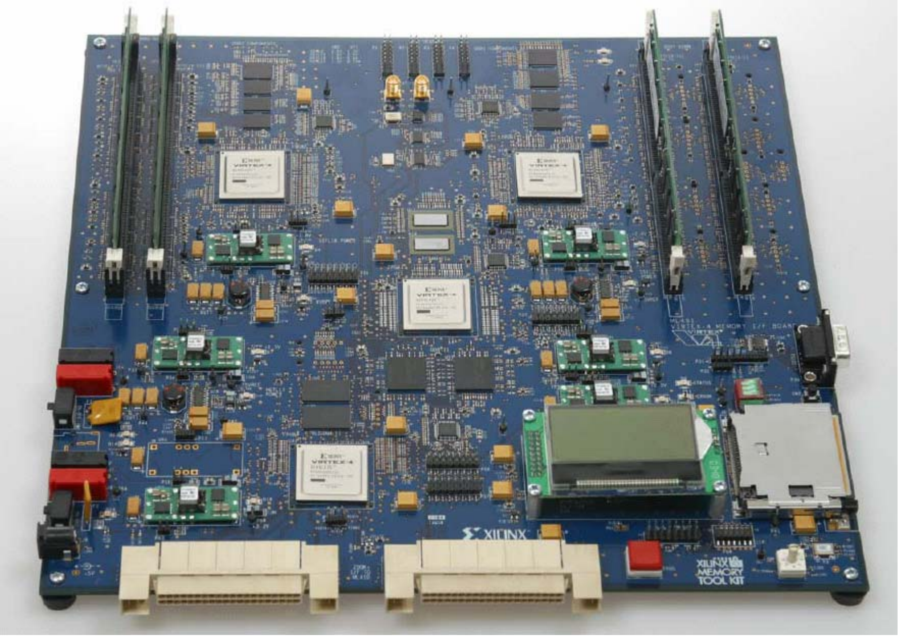
Multiple Designs Simulated and Verified in Hardware

- ML461 Development System
  - 4 x LX25 devices supporting multiple memory interfaces
  - JTAG interface for ChipScope Pro (in circuit logic analyzer)
  - Reference designs verified on it
- Available now www.xilinx.com/ml461



	DDR2	DDR	QDR II	RLDRAM II	FCRAM II
Data rate	533 Mbps	400 Mbps	1.2 Gbps	600 Mbps	600 Mbps
CLK Rate	267 MHz	200 MHz	300 MHz	300 MHz	300 MHz
Data Width	144 bit (DIMM)	144 bit (DIMM)	(72+72) bit	36 bit	36 bit

Complex Memory Controller Design

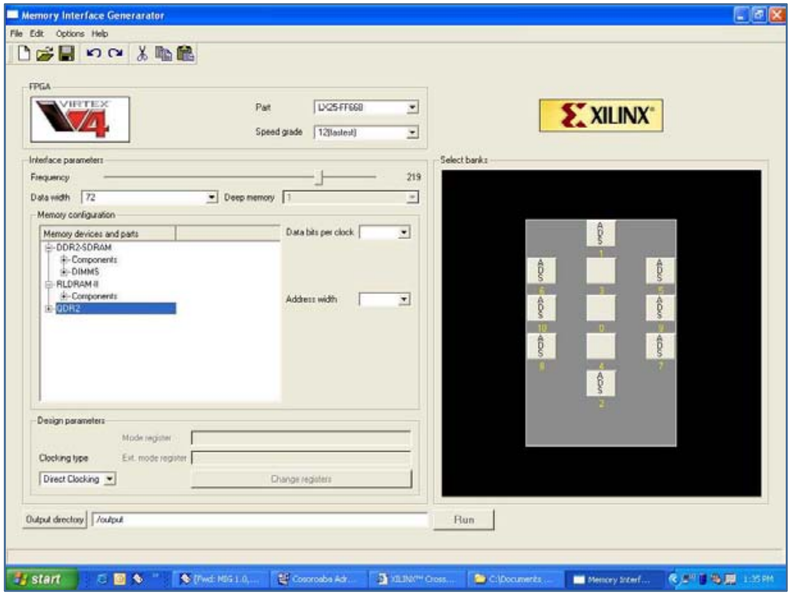
- Controller state machine varies with memory architecture and system parameters
- State machine code to maximize performance involves:
  - Architecture (DDR, DDR2, RLDRAM II, QDR II)
  - Number of Banks (external and internal to the memory device)
  - Data Bus Width (32, 36, 72, etc.)
  - Device width (x4, x8, x9, x16, x18, etc.)
  - Data to Strobe ratios
  - Bank and Page access algorithm

Costly and time-consuming to implement

Memory Interface Generator Makes Design Easy

- Generates :
  - HDL code
  - Constraints file
  - Synthesizable test bench

- **Available now** FREE
  www.xilinx.com/memory

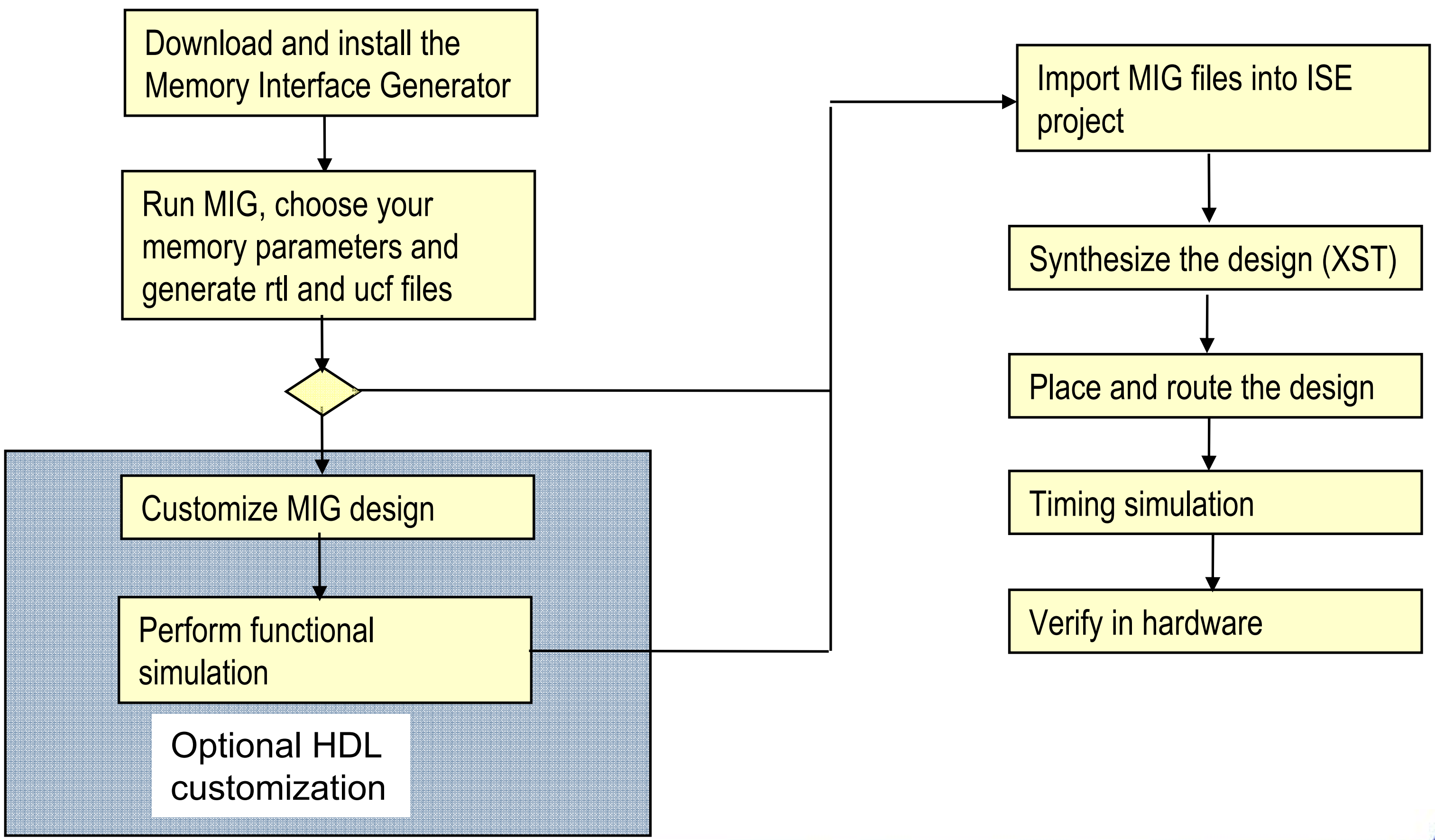


User-friendly GUI

Design your controller with complete flexibility

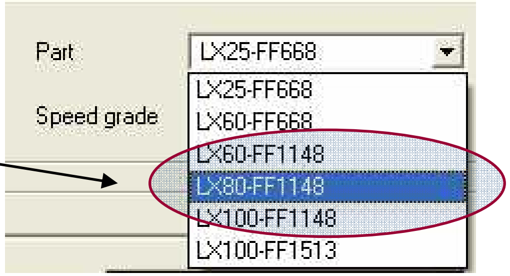
Generates Your Memory Design in Minutes

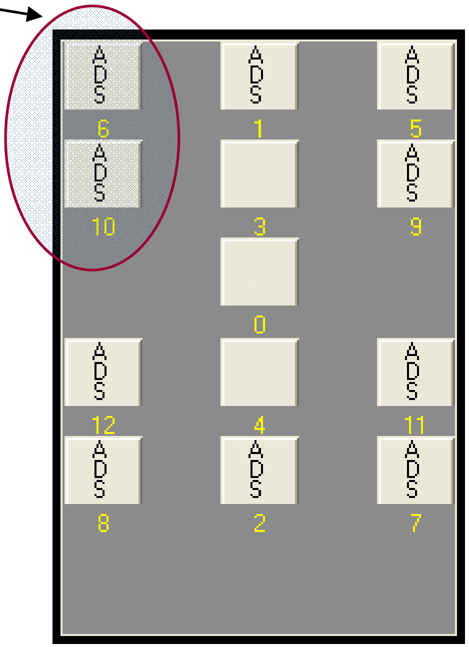
Design Flow

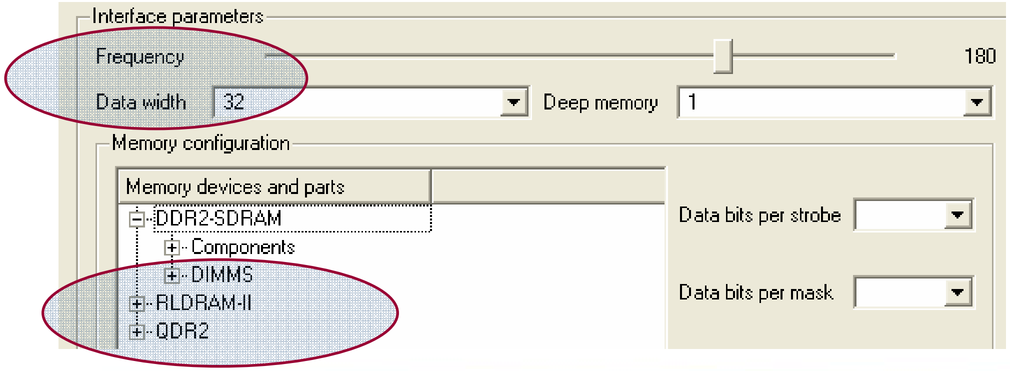


Memory Interface Generator

- Options to select
  - FPGA device, package, speed grade
  - Banks and signals
  - Memory Interface clock freq.
  - Memory architecture and devices (DIMM modules)
  - Data (bus) width and depth







Memory Interface Generator

- Outputs generated from a library of hardware-verified designs
  - Constraints file (ucf)
  - Modular HDL files (rtl)
    - Physical layer (IDELAY)
    - Controller state machine
    - User Interface
      - Read FIFO
      - Write FIFO
    - Synthesizable test bench
- Complete visibility to the HDL code
- Option to further customize the memory controller

Name	Size	Type
addr_gen.v	11 KB	V File
backend_fifos.v	8 KB	V File
backend_rom.v	8 KB	V File
cmp_rd_data.v	9 KB	V File
controller_iobs.v	6 KB	V File
data_gen_8.v	11 KB	V File
data_gen_16.v	11 KB	V File
data_path.v	8 KB	V File
data_path_iobs.v	31 KB	V File
data_tap_inc.v	5 KB	V File
data_write.v	7 KB	V File
ddr2_cmd.v	6 KB	V File
ddr2_controller.v	66 KB	V File
idelay_ctrl.v	3 KB	V File
idelay_rd_en_io.v	6 KB	V File
infrastructure.v	8 KB	V File
infrastructure_iobs.v	9 KB	V File
iobs.v	8 KB	V File
mem_interface_top.v	6 KB	V File
parameters.v	2 KB	V File
RAM_D.v	7 KB	V File
rd_data.v	7 KB	V File
rd_data_fifo.v	10 KB	V File
rd_wr_addr_fifo.v	7 KB	V File
tap_ctrl.v	15 KB	V File
tap_logic.v	15 KB	V File
test_bench.v	9 KB	V File
top.v	16 KB	V File
user_interface.v	8 KB	V File
v4_dm_iob.v	4 KB	V File
v4_dq_iob.v	7 KB	V File
v4_dqs_iob.v	8 KB	V File
wr_data_fifo_8.v	5 KB	V File
wr_data_fifo_16.v	5 KB	V File

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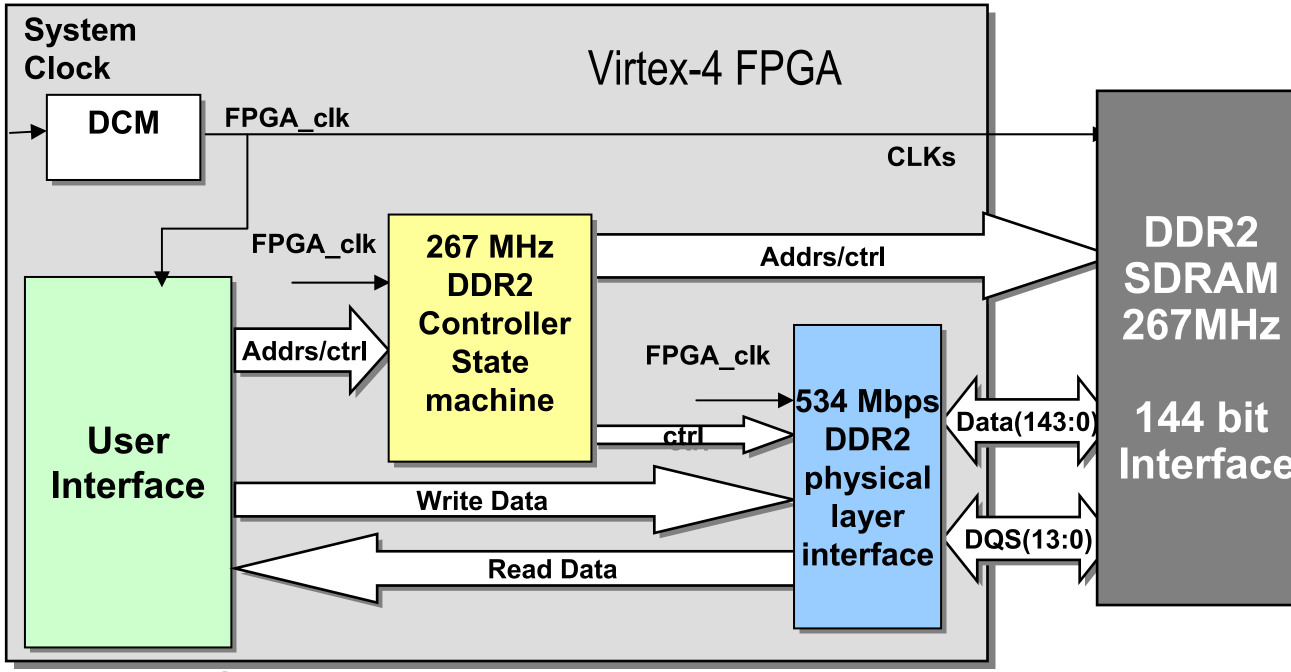
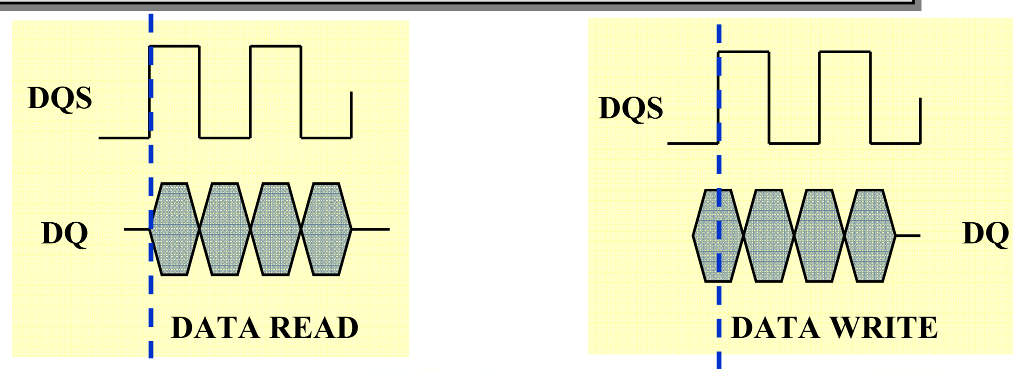
- Memory Trends
- Design Challenges and Solutions
- DDR2 SDRAM Interface
- Summary

267MHz(533 Mbps) DDR2 Interface

- Physical Layer interface
  - Read data and strobe/clock received edge aligned from memory device
  - Write data and strobe/clock transmitted center aligned with each other
- Controller
- User Interface





Physical Layer - Read

- Traditionally challenging read data physical layer is made easier with Virtex-4
- Direct Clocking Technique
  - DQS memory strobe used to determine data delay value
  - Read data delayed to center align to FPGA clock, CLK0
  - Read data captured directly in CLK0 domain using Input DDR Flip Flops

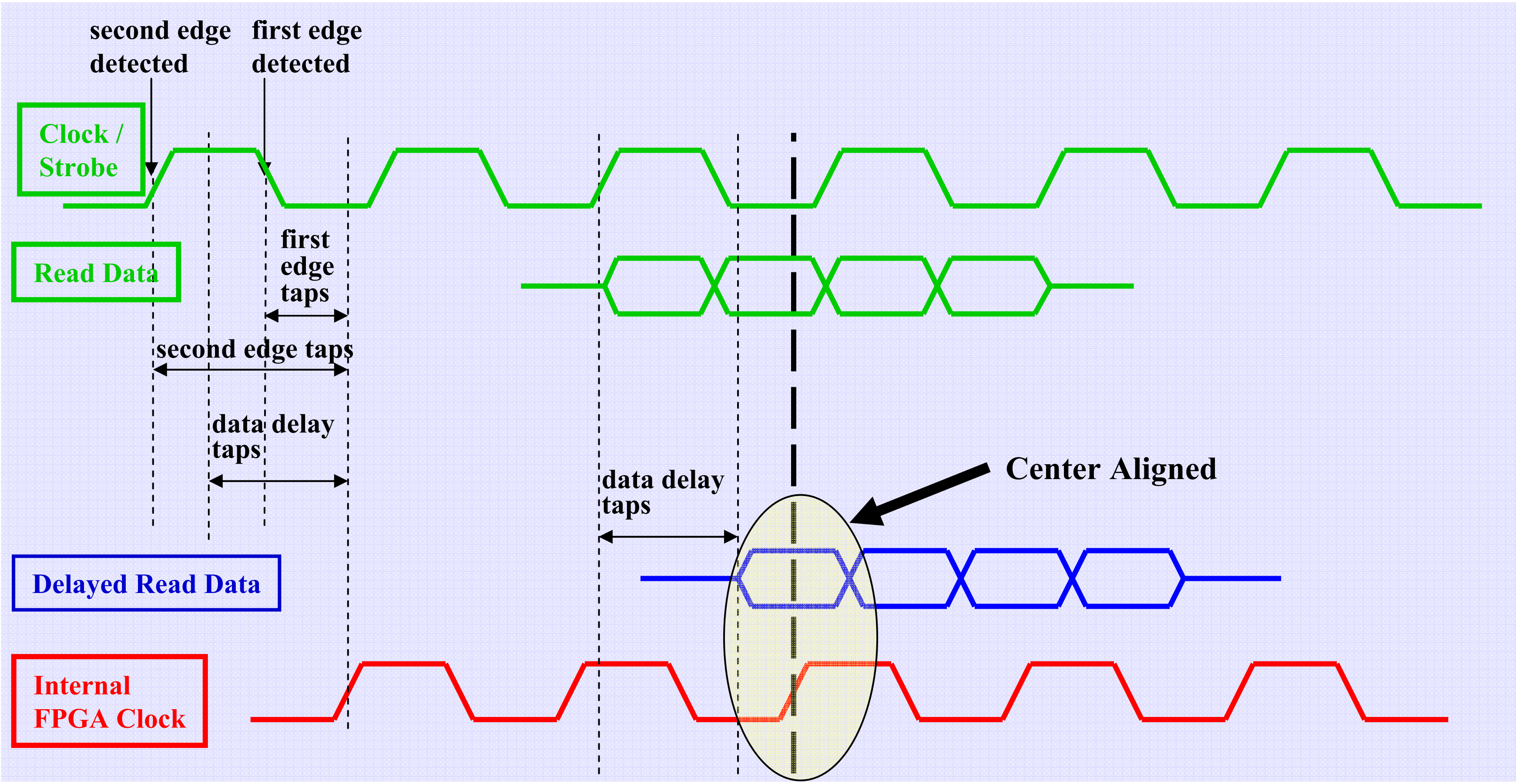
Data-to-clock centering for every DQS signal

Data-to-Clock Centering

- Executed at "run time" during initialization
- Memory strobe input to IDELAY block (part of ChipSync) set to 0 taps
- Output of IDELAY block registered using FPGA clock, CLK0, for edge detection
  - Number of taps required to detect first edge recorded
  - Number of taps required to detect second edge recorded
  - Difference between first edge taps and second edge taps is pulse width
  - Required data delay is sum of first edge taps and pulse center

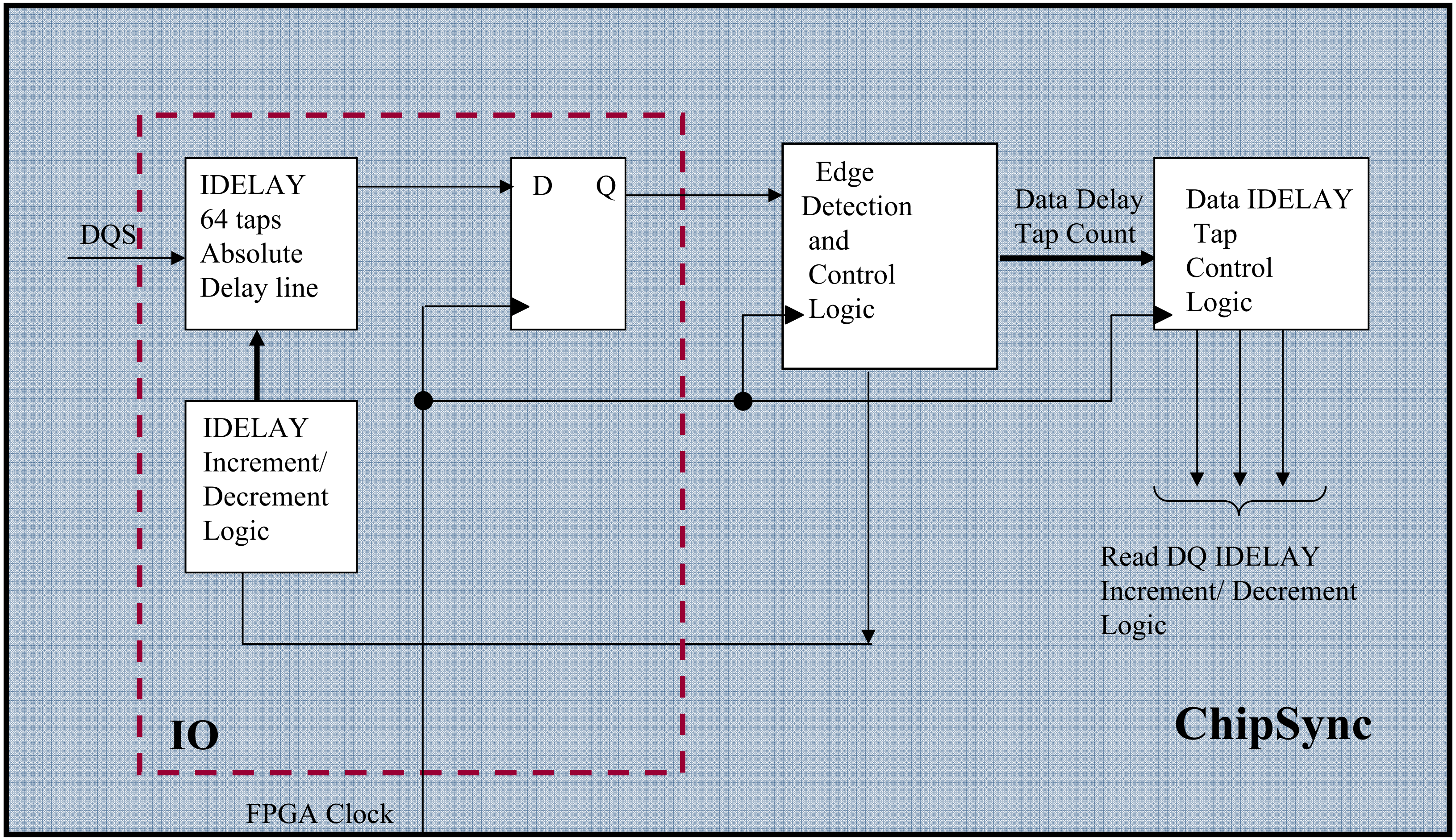
Data-to-clock centering for every DQS signal

Data-to-Clock Centering



"Run time" data-to-clock centering during initialization

Memory Strobe IO Diagram



DQS to FPGA clock phase shift detection

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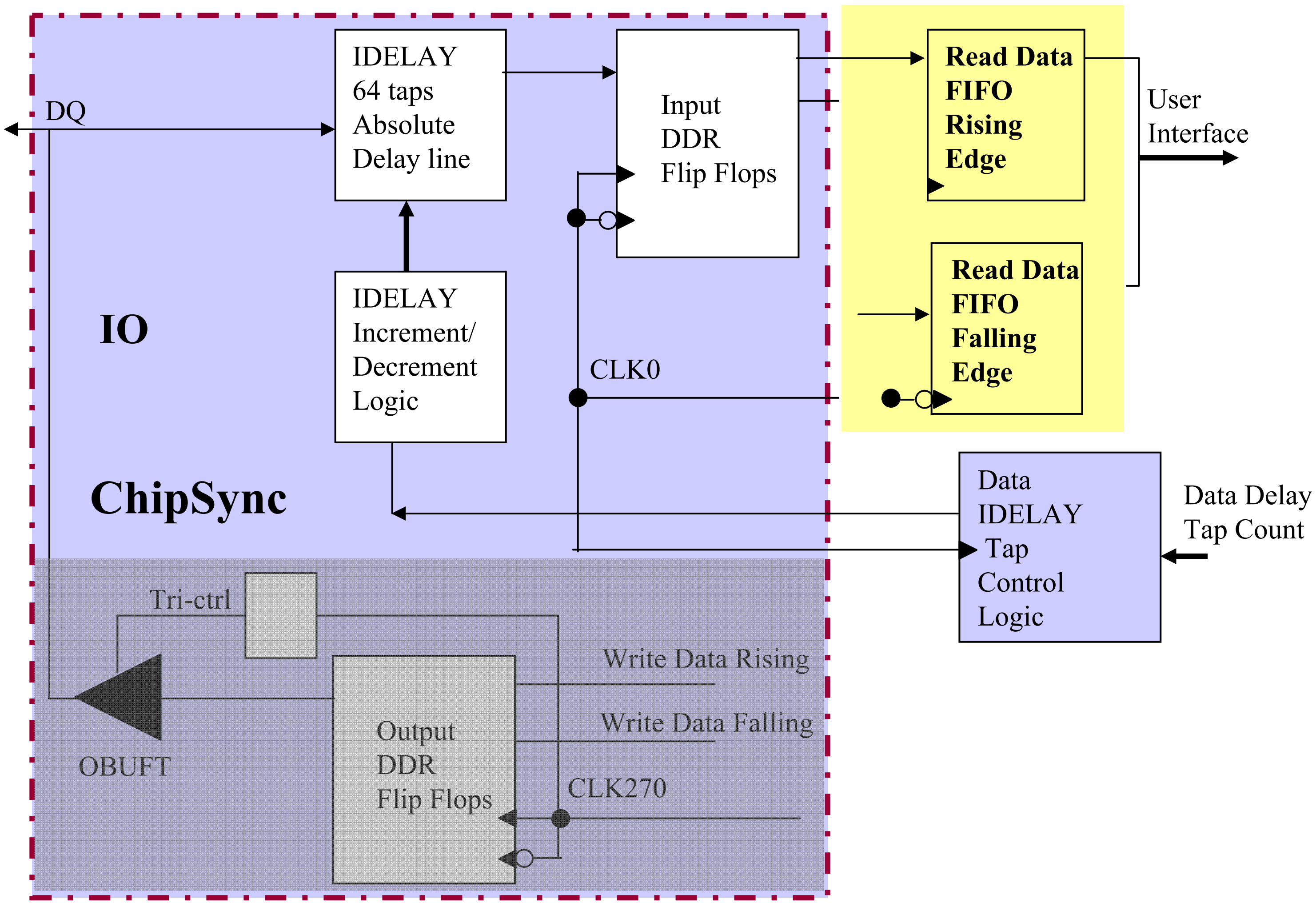
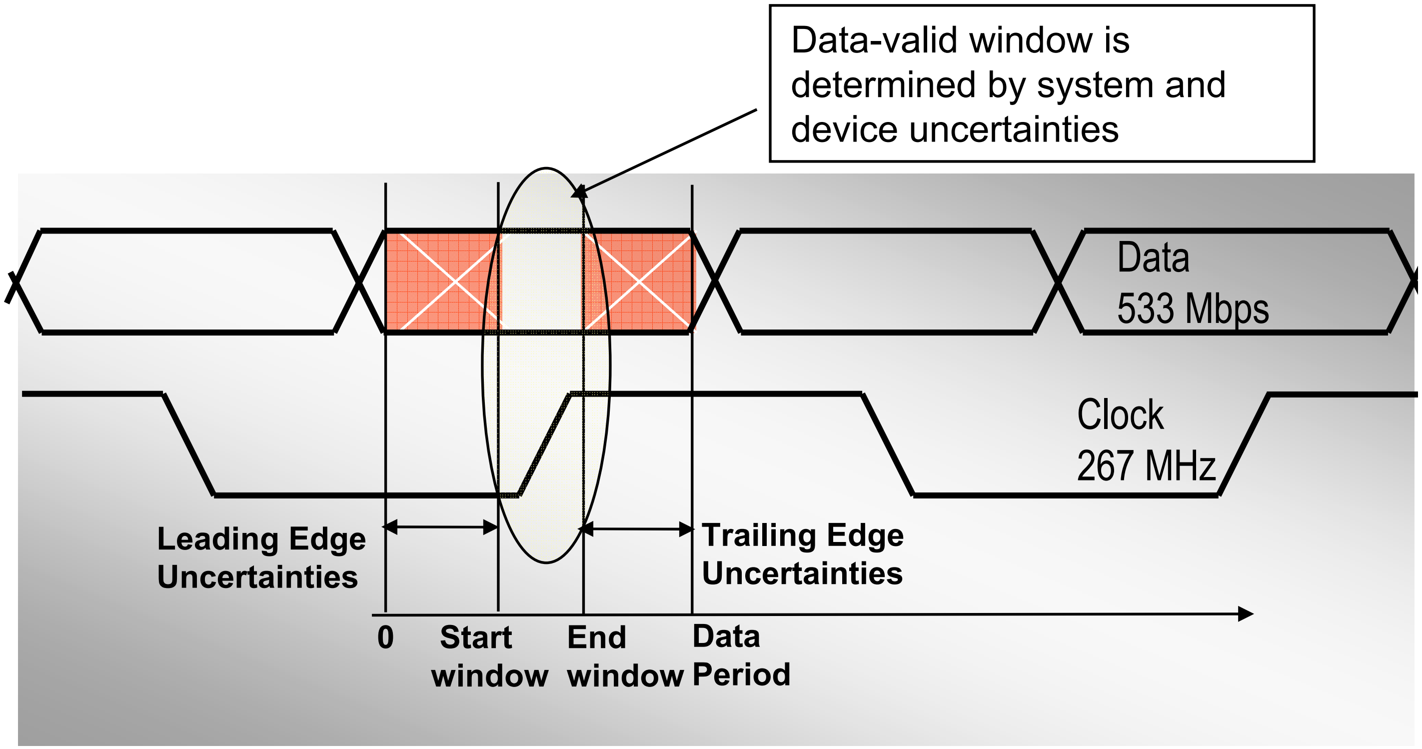
Read Data Path Diagram



Data inputs delayed and captured in FPGA clock domain

Timing Margin Analysis



DDR2 Read Timing @ 267 MHz

Parameters	Value(ps)	Uncertainities before DQS	Uncertainities after DQS	Meaning
Tclock	3750			Clock period
Tmemory_dll_duty _cycle_dist	188	188	188	Duty cycle distortion from memory DLL is subtracted from half clock period to determine Tdata_period.
Tdata_period	1687			Data period is half the clock period with 10% duty cycle distortion subtracted from it.
Memory uncertainties(Tac)	500	500	500	This parameter considers the worst of all the memory parameters. Tac = 500ps for 267 MHz.
Tpackage_skew	30	15	15	Package skew
Tsetup - Min	0	0	0	DQS edge detection is performed by registering it in the IO flip flop with a global clock. The final data delay value therefore already accounts for the setup and hold times of the IO flip flops. Hence these parameters are not considered in this
Thold - Max	0	0	0	
Tjitter	100	100	100	Clock jitter that indirectly causes strobe jitter
Tclock_tree_skew - Max	50	50	50	Small value considered for Skew on "global clock" line since detection of DQS and associated DQ are placed close to each other
Tpcb_layout_skew	20	20	20	Skew between data lines and associated strobe on the board
Uncertainties		685	685	
Window	**317**	**685**	**1002**	

Data-valid window is more than 2 x the 78 ps tap resolution

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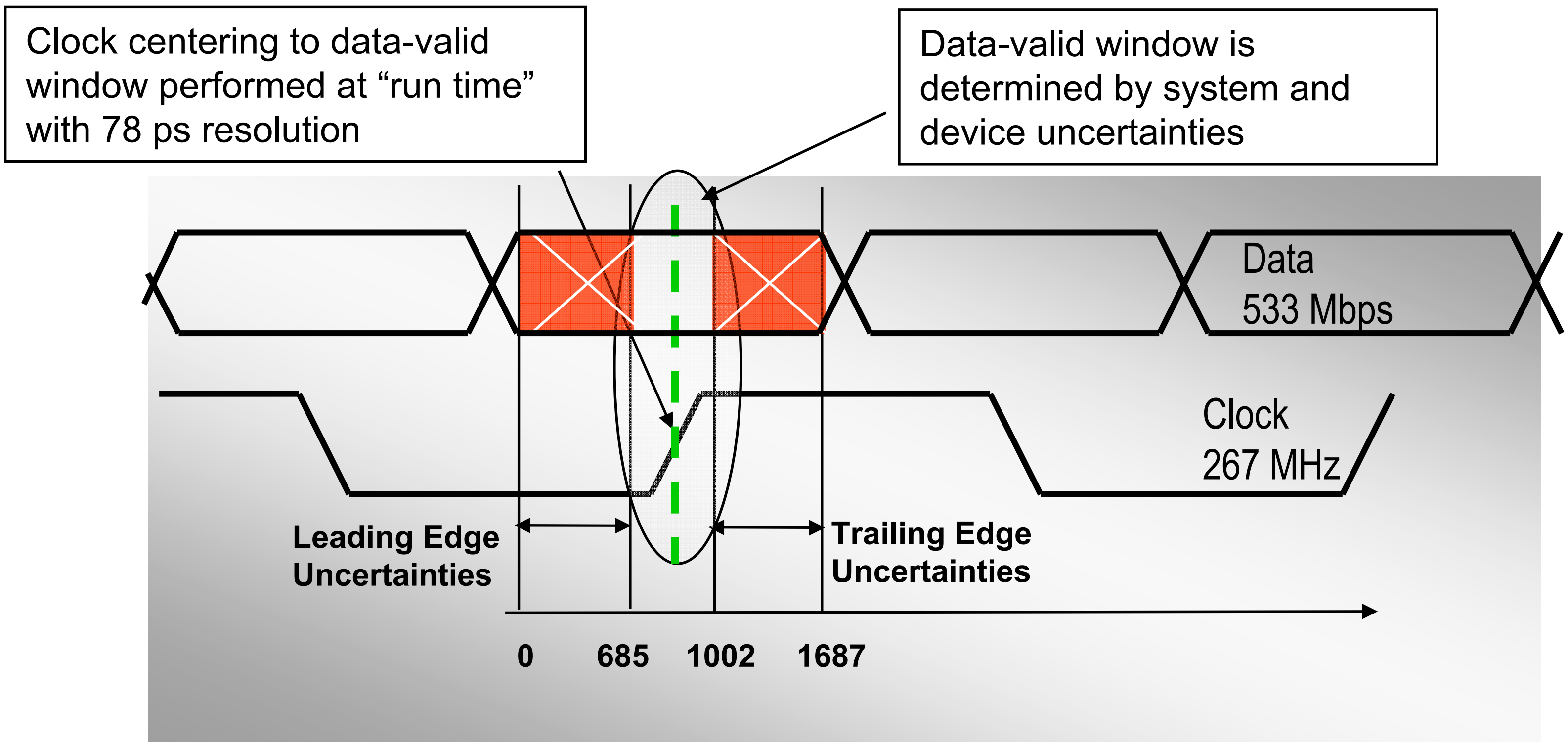
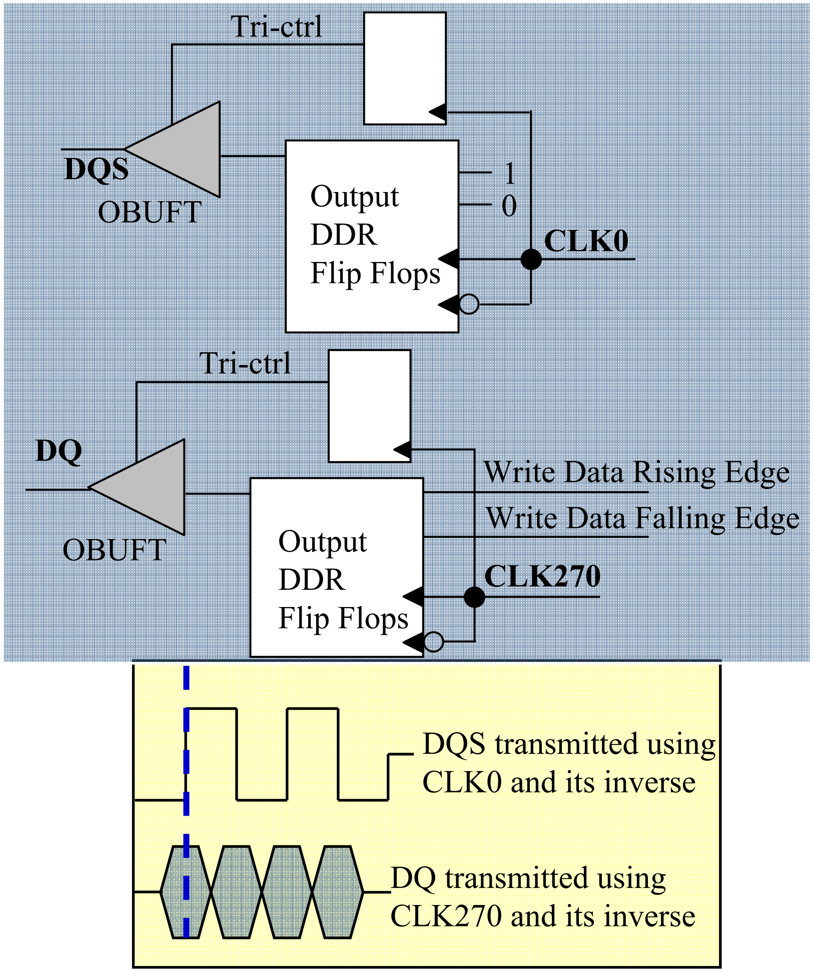
DDR2 Read Timing @ 267 MHz



Data-valid window is more than 2 x the 78 ps tap resolution

Write Data Path

- Write data path easy to implement due to DCM and Output DDR
- Write strobe/clock must be center aligned with data
- Write strobe/clock generated using Output DDR clocked by CLK0 DCM output
- Write data transmitted using Output DDR clocked by CLK270 DCM output



Data outputs center aligned with DQS

DDR2 Write Timing @ 267 MHz

Parameters	Value(ps)	Uncertainities before DQS	Uncertainities after DQS	Meaning
Tclock	3750			Clock period
Tmemory_dll_duty_cycle_dist	188	188	188	Duty cycle distortion from memory DLL subtracted from half clock period to determine Tdata_period.
Tdata_period	1687			Data period is half the clock period with 10% duty cycle distortion subtracted from it.
Tsetup	100	100	0	Only the worst case parameter Tac being considered.
Thold	225	0	225	Only the worst case parameter Tac being considered.
Tpackage_skew	30	15	15	Package skew
Tjitter	0	0	0	Same DCM used to generate DQS and DQ
Tclock_tree_skew - Max	50	50	50	Small value considered for Skew on "global clock" line since detection of DQS and associated DQ are placed close to each other
Tclock_out_phase	140	140	140	Phase offset error between different clock outputs of the same DCM.
Tpcb_layout_skew	20	20	20	Skew between data lines and associated strobe on the board
Uncertainties		325	450	
Window	**912**	**325**	**1237**	

Write data-valid window provides a comfortable margin

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Memory Interface Design Challenges Solved

- 1. Timing critical physical layer
  - Chipsync built in every I/O
    - Clock-to-data centering at "run time"
- 2. High bandwidth system requirements
  - Column-based architecture and superior packaging
  - 600Mbps x 432 bit wide buses
- 3. Complex memory controller design
  - Hardware verified solutions for all popular memory types (DDR2, DDR SDRAM, QDR II SRAM, RLDRAM II)
  - Memory Interface Generator (MIG)
    - Generates your design in minutes

FREE

Virtex-4 Wins!

Memory Interfaces Made Easy

How to Get Started

- Leverage the complete hardware verified solutions to assure first time design success

- Access latest Virtex-4 memory design solutions on www.xilinx.com/memory
  - Memory Interface Generator (MIG)
  - Application Notes
  - ML461 - Advanced Memory Development System
    - Board level solution including: reference designs, schematic & gerber files
    - DDR2, DDR SDRAM, QDR II SRAM,RLDRAM II, FCRAM II

FREE

- Contact your local FAE for an on-site demo

Accelerate Your Design Cycle