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### **Project Name: vgaStripes**

Creation Date: May 2003

Development Board: XESS XSA-100 Plus XStend Version 2

Development Software: Xilinx ISE Version 5.1.03i

#### Description

This project generates a vga signal and displays a set colored bars on a monitor.

The XStend board is not needed in this project, except for the fact that I possibly still have some pin references to it.

**The XSA-100 board frequency must be set to 25MHz!**

#### Project Directory Structure

This project is organized into the following directories:

./ - contains all the files need to synthesize the design.

./config – effectively a backup of all main files in the root directory

./docs – this PDF file. Source files used to build this PDF are located in ./docs/src.

./src – source directory for all HDL files

./temp – temporary directory used during the build process.

#### Synthesis

The project is built and maintained using two windows based batch files. The first is “make.bat”. It simply issues the commands required to “compile” all the source files in the ./src directory and eventually generate the chipIO.bit file to downloaded to the fpga.

The second batch file is called “clean.bat”. Its sole purpose is to delete most of the unwanted files generated during the build process.

## References

Primary reference in building this project, specifically the vga signal generation circuit was the book titled “Rapid Prototyping of Digital Systems – A Tutorial Approach Second Edition”. I highly recommend this book for a collection of great design experiments!