Department of Electrical and Computer Engineering
COEN 312 Dec.15, 2009
Answer all Questions. All questions carry equal marks.
Exam Duration 3 hour
Examiners: Asim J. Al-Khalili, Shah Jahinuzzaman
No books / papers or electronic devices are allowed.

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Question 1

a)Given F1 and F2 below, determine F1 • F2 and F1 + F2 (3 Marks)

F1= AB + C,
F2= A'C' + B'C'

b) Minimize the following Boolean Function: (3 Marks)

F(A,B,C,D)= ABC' + BC'D' + AC'D + ABC + BCD' + ACD'

c) Given f(A,B,C) = AB +A C' + BC (4 Marks)

i) Implement f in **NOR-NOR** format
ii) Implement f in **AND-OR-INVERT** format
Obtain optimum implementation.

Question 2

a) Design a combinational circuit that implements (8 Marks)

$F= 2t^2-2$

t can take the integer values of 1 or 2 **only**.
Show your design steps clearly starting with the Truth Table.
Draw the final circuit.

b) If the function is to be implemented on a ROM what size of ROM is required?
(2 Marks)

Question 3

a) Design a 1-bit full adder. Clearly show the truth table and logic diagram. (4 Marks)

b) Use a 1-bit full adder plus extra logic if required to design a 4-bit **serial subtractor** for unsigned numbers. The full adder can be assumed as a block having two 1-bit inputs, A and B, an input carry, an output SUM, and an output CARRY. (6 Marks)

Question 4

a) Use 2 to 1 MUXes to build a 4 to 1 MUX. (2Marks)

b) Use a 8 to1 MUX to implement F (2 Marks)

F(A,B,C,D)= ABC' + BC'D' + AC'D + ABC + BCD' + ACD'

c) Use a 4 to1 MUX plus minimal extra logic to implement F. (4 Marks)

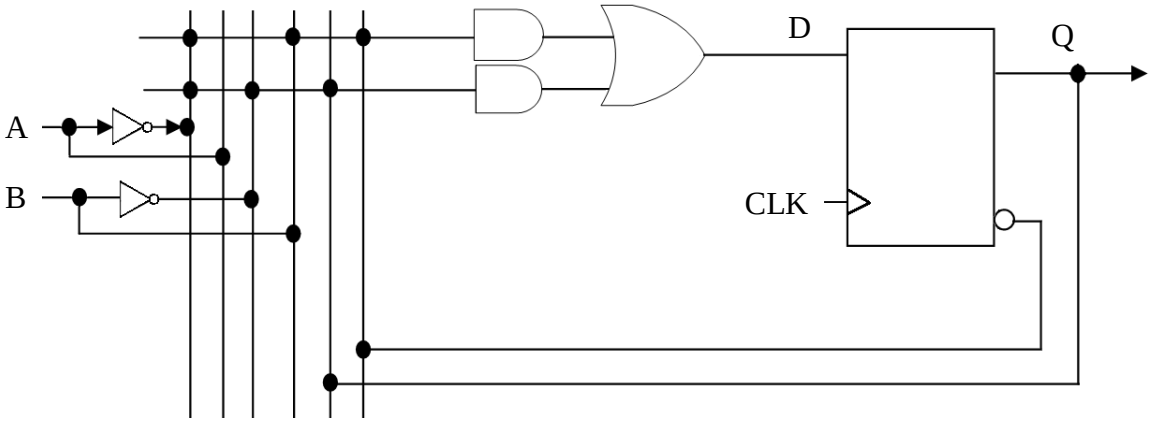
d) What is the delay of the circuit if any gate has a delay of d. Take the internal structure of the MUX into account. (2 Mark)

Question 5

Design an **UP/DOWN BCD** counter, starting with a state diagram. Use D-Flip Flop for your implementation. (10 Marks)

Question 6

The sequential circuit given below uses a PAL to implement the combinational logic. Analyze the circuit below fully. Derive the Transition Table, Excitation Table, State Diagram and the Output. (8 Marks)
State what the function does. (2 Marks)



Q1

a) $F1 = AB + C$, $F2 = A'C' + B'C'$

$F1 \cdot F2 =$ $(AB + C)(A'C' + B'C') = 0$

$F1 + F2 =$
$AB + C + A'C' + B'C'$
$AB + (C + A')(C + C') + B'C'$
$AB + C + A' + B'C'$
$(A' + A)(A' + B) + (C + B')(C + C')$
$A' + B + C + B'$
1

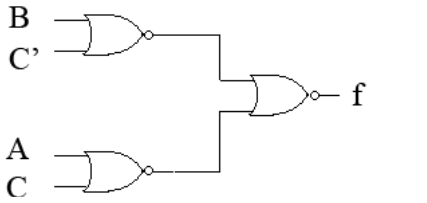
b)
$F = ABC' + BC'D' + AC'D + ABC + BCD' + ACD'$
$F = AB(C' + C) + BD'(C' + C) + AC'D + ACD'$
$F = AB + BD' + AC'D + ACD'$

c) $f = AB + AC' + BC$
Apply consensus $f = AC' + BC$

i) NOR-NOR

$f' = (A' + B')(A' + C)(B' + C')$
$f' = (A' + A'B' + A'C + B'C)(B' + C')$
$f' = (A'B' + A'B'C + B'C + A'C' + A'B'C')$
$f' = A'B' + B'C + A'C'$

$\therefore f = (A'B' + B'C + A'C')'$
$f = [(C + C') + (B + C')' + (A + C)']'$ (consensus)

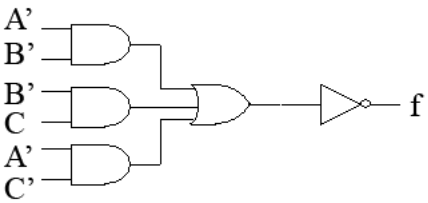


C/AB	0	1	11	10
0	0	0	1	1
1	0	1	1	0

(A+C)(B+C')

ii) AND-OR-INVERT

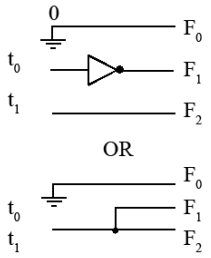
$f' = A'B' + B'C + A'C'$
$f = (A'B' + B'C + A'C')'$



Q2

a) $F = 2t^2 - 2$, t=1 or 2 only, so maximum input width 2bits (00 or 10) with t=2, F=2.2^2-2=6, so maximum output width 3bits

t_1	t_0		F_2	F_1	F_0
0	0	-	x	x	x
0	1	-	0	0	0
1	0	-	1	1	0
1	1	-	x	x	x

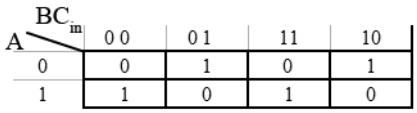


b) ROM size: 4 x 3

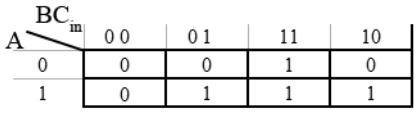
Q3

a) Full adder: Inputs A, B, Cin
Outputs S, Cout

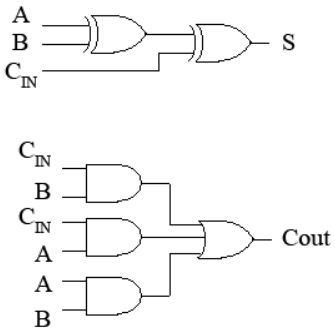
A	B	Cin		S	Cout
0	0	0	-	0	0
0	0	1	-	1	0
0	1	0	-	1	0
0	1	1	-	0	1
1	0	0	-	1	0
1	0	1	-	0	1
1	1	0	-	0	1
1	1	1	-	1	1

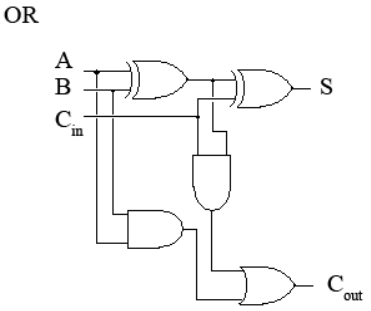


$$S = A \oplus B \oplus C_{in}$$



$$C_{out} = BC_{in} + AC_{in} + AB$$
$$= AB + C_{in}(A \oplus B)$$

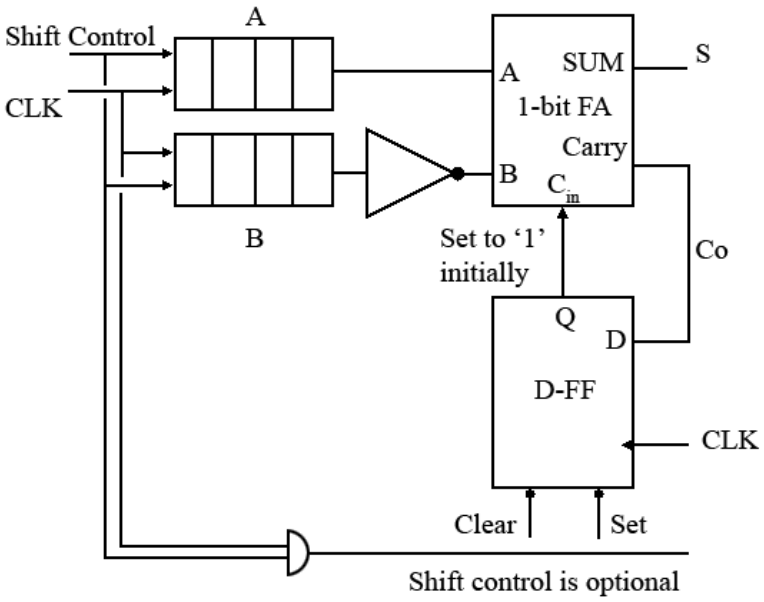




Q3

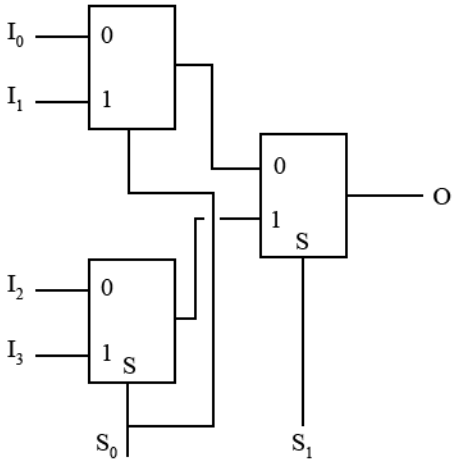
b)

Substraction can be done using the addition of two operands when one of the operands is in 2's complement form. 2's complement of an operand can be obtained by inverting all the bits and adding a 1 to the operand. In a full adder, the addition of 1 to the inverted bits can be done by setting the input carry to 1. For a serial adder, the input carry should be 'set' to 1 only at the first clock cycle.



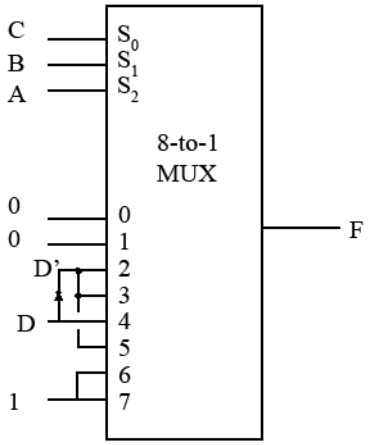
Q4

a) 4-to-1 MUX from 2-to-1 MUX



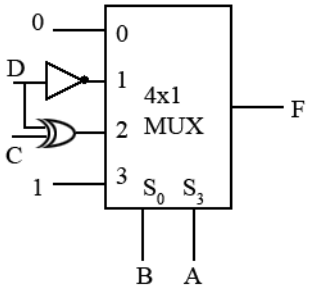
b) $F = AB\overline{C} + B\overline{C}\,\overline{D} + A\overline{C}D + ABC + BC\overline{D} + AC\overline{D}$

A	B	C	D	F	
0	0	0	0	0	F = 0
0	0	0	1	0	
0	0	1	0	0	F = 0
0	0	1	1	0	
0	1	0	0	1	F = D’
0	1	0	1	0	
0	1	1	0	1	F = D’
0	1	1	1	0	
1	0	0	0	0	F = D
1	0	0	1	1	
1	0	1	0	1	F = D
1	0	1	1	0	
1	1	0	0	1	F = 1
1	1	0	1	1	
1	1	1	0	1	F = 1
1	1	1	1	1	



c)

A	B	C	D	F	
0	0	0	0	0	AB = 0
0	0	0	1	0	F = 0
0	0	1	0	0	
0	0	1	1	0	
0	1	0	0	1	AB = 01
0	1	0	1	0	F = C’D’+CD’
0	1	1	0	1	= D’
0	1	1	1	0	
1	0	0	0	0	AB = 10
1	0	0	1	1	F = C’D+CD’
1	0	1	0	1	$= C \oplus D$
1	0	1	1	0	
1	1	0	0	1	AB = 11
1	1	0	1	1	F = 1
1	1	1	0	1	
1	1	1	1	1	

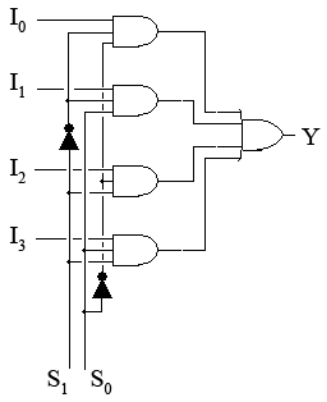


d)

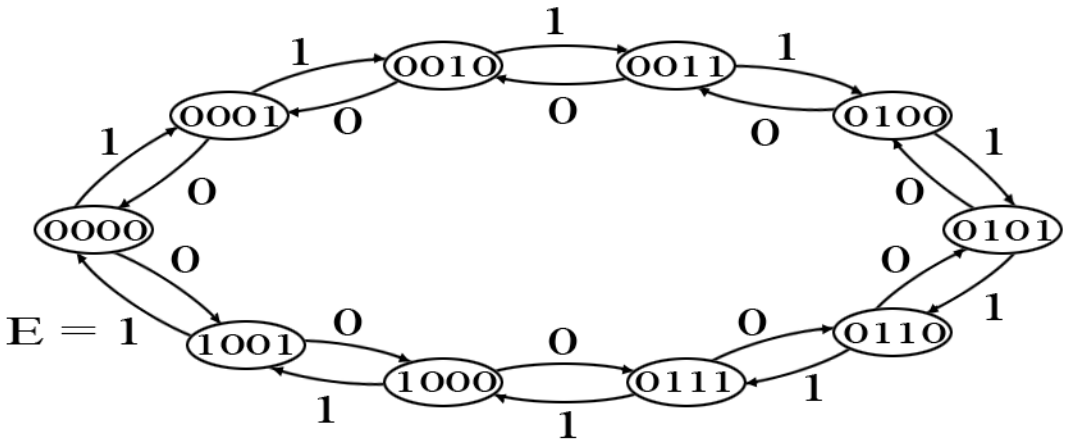
To calculate the delay, we consider the internal structure of the 4-to-1 MUX:
So for the above circuit implementation with MUX, the number of gates is:

From A to F = 3
From B to F = 3
From C to F = 3
From D to F = 3

So the worst case delay = 3 gate delays = 3d.

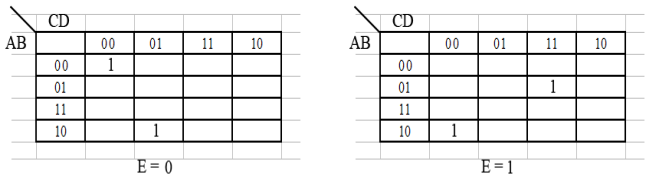
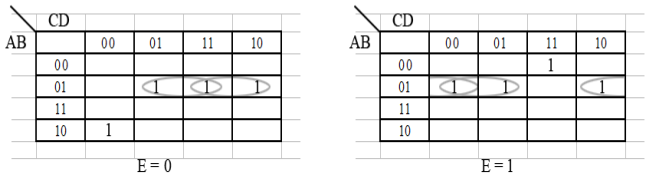


Q5) Up/Down BCD counter



Control	Present State					Next State					Flip-Flop Inputs			
E	A	B	C	D		A	B	C	D		D_A	D_B	D_C	D_D
0	0	0	0	0		1	0	0	1		1	0	0	1
0	0	0	0	1		0	0	0	0		0	0	0	0
0	0	0	1	0		0	0	0	1		0	0	0	1
0	0	0	1	1		0	0	1	0		0	0	1	0
0	0	1	0	0		0	0	1	1		0	0	1	1
0	0	1	0	1		0	1	0	0		0	1	0	0
0	0	1	1	0		0	1	0	1		0	1	0	1
0	0	1	1	1		0	1	1	0		0	1	1	0
0	1	0	0	0		0	1	1	1		0	1	1	1
0	1	0	0	1		1	0	0	0		1	0	0	0
0	x	x	x	x		0	0	0	0		0	0	0	0
1	0	0	0	0		0	0	0	1		0	0	0	1
1	0	0	0	1		0	0	1	0		0	0	1	0
1	0	0	1	0		0	0	1	1		0	0	1	1
1	0	0	1	1		0	1	0	0		0	1	0	0
1	0	1	0	0		0	1	0	1		0	1	0	1
1	0	1	0	1		0	1	1	0		0	1	1	0
1	0	1	1	0		0	1	1	1		0	1	1	1
1	0	1	1	1		1	0	0	0		1	0	0	0
1	1	0	0	0		1	0	0	1		1	0	0	1
1	1	0	0	1		0	0	0	0		0	0	0	0
1	x	x	x	x		0	0	0	0		0	0	0	0

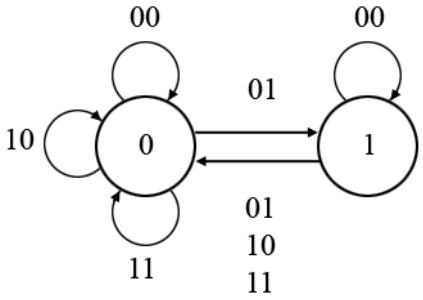
b)

DA		$D_A = E'(A'B'C'D' + AB'C'D) + E(AB'C'D' + A'BCD)$
DB		$D_B = E'(A'BD + A'BC + AB'C'D') + E(A'BC' + A'BD' + A'B'CD)$

Q6)

Q(t)	A	B		Q(t+1)	D
0	0	0	-	0	0
0	0	1	-	1	1
0	1	0	-	0	0
0	1	1	-	0	0
1	0	0	-	1	1
1	0	1	-	0	0
1	1	0	-	0	0
1	1	1	-	0	0

$$D_A = Q'A'B + QA'B'$$
$$= A'(Q'B + QB')$$
$$= A'(Q \oplus B)$$



Whenever A=0 & Q not equal to B, output becomes '1' on next state

Q	A	B	
0	0	0	Hold State
1	0	0	
0	0	1	Toggle State
1	0	1	
0	1	X	Reset
1	1	X	