**COEN 6501 Digital design and Synthesis**

Oct. 19, 2015 Lecturer: Asim J. Al-Khalili

Answer all Questions. All Questions carry equal marks

Exam Duration: 1hr 30 min.

No books, papers or calculators are allowed.

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**Question 1**

Give an architecture that can calculates

**F = 2XY -5**

where X, Y are 4-bit unsigned numbers. Show all inputs/outputs and the critical path clearly.

Test your circuit with X= 0101, and Y= 0011

**Question 2**

Represent the numbers “7.25” and “-0.75” in IEEE 754 floating point format.

Multiply these numbers and show your steps.

Give an architecture for floating point multiplication.

What methodology is used for rounding in IEEE 754. Explain the method, and give its advantage and disadvantages

**Question 3**

What are the advantages and disadvantages of Carry Select Adders.

Use Carry Select adder to implement optimally the addition of two 17 bit unsigned numbers.

Calculate the delay and area in terms of Full adders and Muxes of your design.