11 Finite State Machine (SSN sequencer)

NOTE: The PRELAB for this lab has Altera MAXPLUS simulation requirements. See the Prelab sheets for more information.

I. Overview

A finite state machine is a digital system that can be characterized by a finite number of states, with transitions between states controlled by the present state and current input values. The output of the FSM will be a function of the current inputs and present state.

In this lab you will design a finite state machine whose sequencing is based upon your SSN number. You will need to look at the following link:

- http://www.ece.msstate.edu/~reese/EE3714/ssnseq/index.htm

To compile your VHDL, you will need use the following link:

- http://www.ece.msstate.edu/~reese/EE3714/webcad/ssnseqlab.htm

II Report

You need to include your ASM chart and the complete derivation of your boolean equations for your FSM. Also have the printout of the successful VHDL compilation/simulation of your design from the WWW, and also a screenshot of the Altera MAXPLUS simulation of your VHDL file. Be sure to JUSTIFY the Altera simulation results (i.e., how to do you know that these results are correct???)

PRE LAB DATA SHEET TA CHECKOFF _____

The majority of the work done in lab is done within the prelab. You MUST have a copy of your successful VHDL compilation/simulation of your FSM when you walk into lab.

A. ASM Chart for your design.

B. Boolean equations for your design.

C. Successful WWW VHDL compilation/simulation of the design.

D. Successful Altera Maxplus VHDL simulation of your design (screenshots or active demo to TA). The attached ZIP file on the WWW page gives a sample VHDL implementation and a simulation waveform that can be used to test the design.

LAB DATA SHEET

A. Working PLD implementation of FSM?

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