ChipPlanner v5.0
User's Guide

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Trademarks

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Introduction

ChipPlanner is a graphical application for viewing and placing I/O and logic macros. You can also use it for floorplanning. This tool is particularly useful when you need maximum control over your design placement.

Note: ChipPlanner does not support ACT1, ACT2, ACT3, MX, DX, eX, SX, SX-A. Use ChipEditor instead.

Use ChipPlanner to:

- View macro placements made during layout
- Place, unplace, or move macros
- Fix I/O macro placements
- View net connections using a ratsnest or route view
- View architectural boundaries
- View and edit silicon features, such as I/O banks
- Cross probe with Silicon Explorer to select probes
- View placement and routing of paths when used with Timer
- Create and assign macros or nets to regions

Starting, Committing, and Exiting

Starting and Exiting ChipPlanner

To start ChipPlanner:

1. If you have not done so, Compile your design.
2. From the **Tools** menu, click **ChipPlanner.** The MultiView Navigator starts with ChipPlanner active.

Tip: You can also start ChipPlanner by clicking ChipPlanner in the Designer design flow window

Exiting ChipPlanner:

1. From the **File** menu, click **Close**.
2. To close the MultiView Navigator, from the **File** menu, click **Exit**.

Committing

Changes made are not permanent until you use the Commit command. The Commit command saves your changes to your design session. Changes are not reversible. To permanently save your changes, you must save your design in Designer.

To commit your changes:

1. From the **File** menu, click **Commit**.

Logic Assignment

About assignment

Manually assigning logic is an optional methodology to help you improve the performance and density of your design.

Assigning and unassigning logic in ChipPlanner

You do not need to manually assign logic in your design. However, should you have specific design requirements, ChipPlanner allows you to have maximum control over your design.

To assign logic using ChipPlanner:

1. Select the logic in the Physical tab.
2. Drag the logic to the desired location. As you drag, valid assignment locations are highlighted. To remove the assignment, from the **Edit** menu, click **Undo**.

   If the logic assignment is valid, the logic is assigned and locked. To save changes for this design session, commit your changes when exiting the MultiView Navigator.

   Note: Assigning logic to a location that already has logic unassigns the previously assigned logic, even if its assignment was locked.

To assign multiple logic macros:

1. While holding down the CTRL or SHIFT key, select the logic in the order you want it placed.
2. From the **Edit** menu, click **Assign**.
3. One by one, select the desired location. The macros are placed in the order selected.

To unassign logic:

1. Select the logic.
2. From the **Edit** menu, click **Unassign.**

To unassign multiple logic macros:

1. Hold down the CTRL or SHIFT key and select the logic you want to unplace. To select all logic, choose **Select All** from the **Edit** menu.
2. From the **Edit** menu, click **Unassign**.

Moving logic

You can move logic that was assigned manually or automatically during Layout.

To move logic:

1. Select the logic.
2. Drag the logic to the new location.

Tip: To remove the placement, from the Edit menu, click Undo.

Locking logic

Locked logic is not moved during Layout. Locked logic only becomes permanent if you commit the changes to your design before exiting.

To lock macros:

1. Select the macro to lock. To select multiple macros, hold the CTRL key and select multiple macros with your mouse. To select all macros, choose Select All from the Edit menu.
2. From the **Logic** menu, click **Lock**.
3. From the **File** menu, click **Commit** to make the changes permanent and update your .adb file.

To unlock a macro:

1. Select the macro. To select multiple macros, hold the CTRL key and select multiple macros with your mouse. To select all macros, from the **Edit** menu, click **Select All**.
2. From the **Logic** menu, click **Unlock**.

Floorplanning

About floorplanning

Floorplanning is an optional methodology that can be used to improve the performance and routability of your design. The objective in floorplanning is to assign logic to specific regions on the chip in order to enhance performance and routability.

When floorplanning, you analyze your design to see if certain logic can be clustered within regions. This is especially helpful for hierarchical designs with plenty of local connectivity within a block. If your timing analysis indicates several paths with negative slack, try clustering the logic included in these paths into their own regions. This forces the placement of logic within the path closer together and may improve timing.

Use ChipPlanner to help you floorplan. ChipPlanner can be used before and after Layout.

About regions

When floorplanning, you assign logic to regions to improve the design performance. Regions can be created using PDC or GCF files, or by using ChipPlanner. Spine regions can only be created using a PDC or GCF file.

Types of regions

There are four types of regions.

Region Type	Conditions
Empty	No macros can be assigned to an empty region.
Exclusive	Only contains macros assigned to the region. Not supported in ProASIC and ProASIC PLUS.
Inclusive	Can contain macros both assigned and unassigned to the region
Spine	Can either be defined as Exclusive or Inclusive in the PDC or GCF file. Cannot be resized. Can only contain certain types of macros.

Creating regions

Using ChipPlanner, you can create Empty, Exclusive, and Inclusive regions.

To create an empty or inclusive region:

1. From the ChipPlanner **Region** menu click **Create Empty, Create Exclusive, or Create Inclusive**.
2. Drag the mouse over the area where you want the region to be placed.

Editing regions

After creating regions with ChipPlanner, you can name, delete, move, and re-size them.

To name a region:

1. Right-click the region and select **Properties**. The Properties dialog box appears.
2. Type a new region name and click **OK**.

To delete a region:

Right-click on the region and select **Delete**.

To move a region:

Select and drag the region to a new location.

Note: The region cannot be moved if a macro assigned to the region is locked to the location.

To re-size a region:

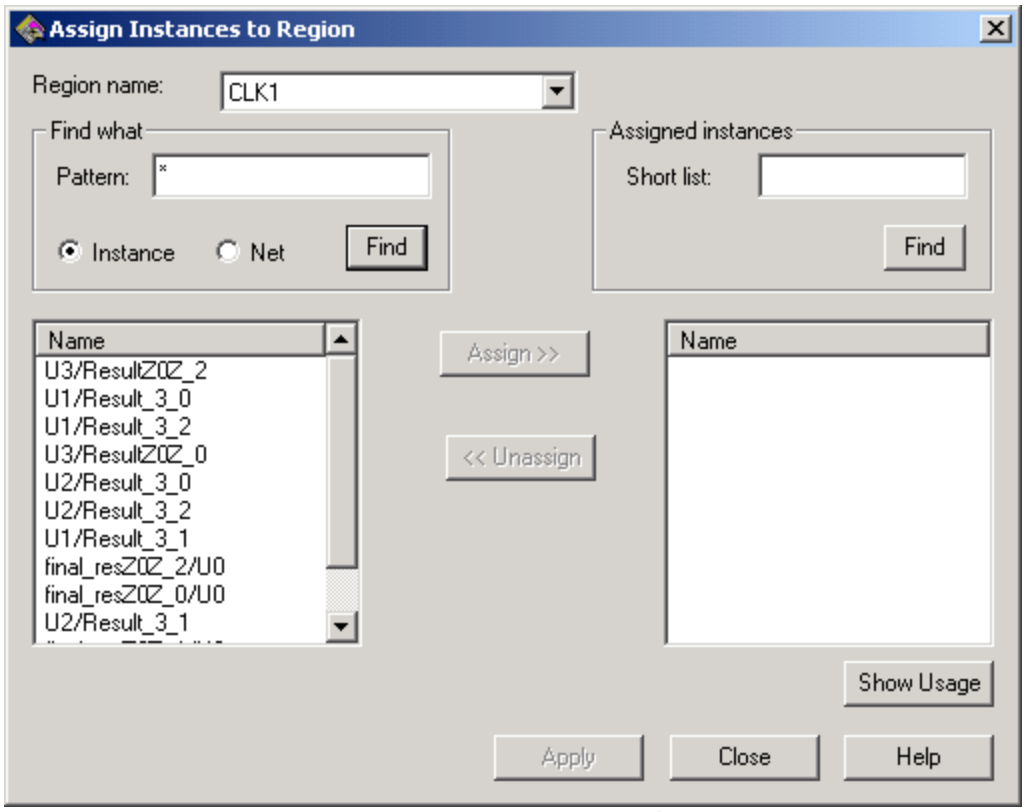
1. Select the region.
2. Grab and drag the sides and corners to re-size the region. A region cannot be re-sized smaller than the logic it already contains.

Assigning logic to regions

During floorplanning, logic can be assigned to regions to improve design performance.

To assign logic to regions:

1. Right-click a region and select **Assign/UnAssign**. The Assign Instances to Region dialog box appears.



Assign Instances to Region Dialog Box

2. Select **Instance**.
3. Enter a Pattern in the text box and click **Find**. To see all instances, type * and click **Find**.
4. Select the instance in the left list box and click **Assign**.

Tip: You can also assign logic to regions by using a drag-and-drop operation.

Assigning nets to regions

When assigning a net to a region, only the instances connected to the net are assigned to the region.

To assign nets to regions:

1. Right-click a region and select **Assign/Unassign**. The Assign Instances to Region dialog box appears.
2. Select **Net**.

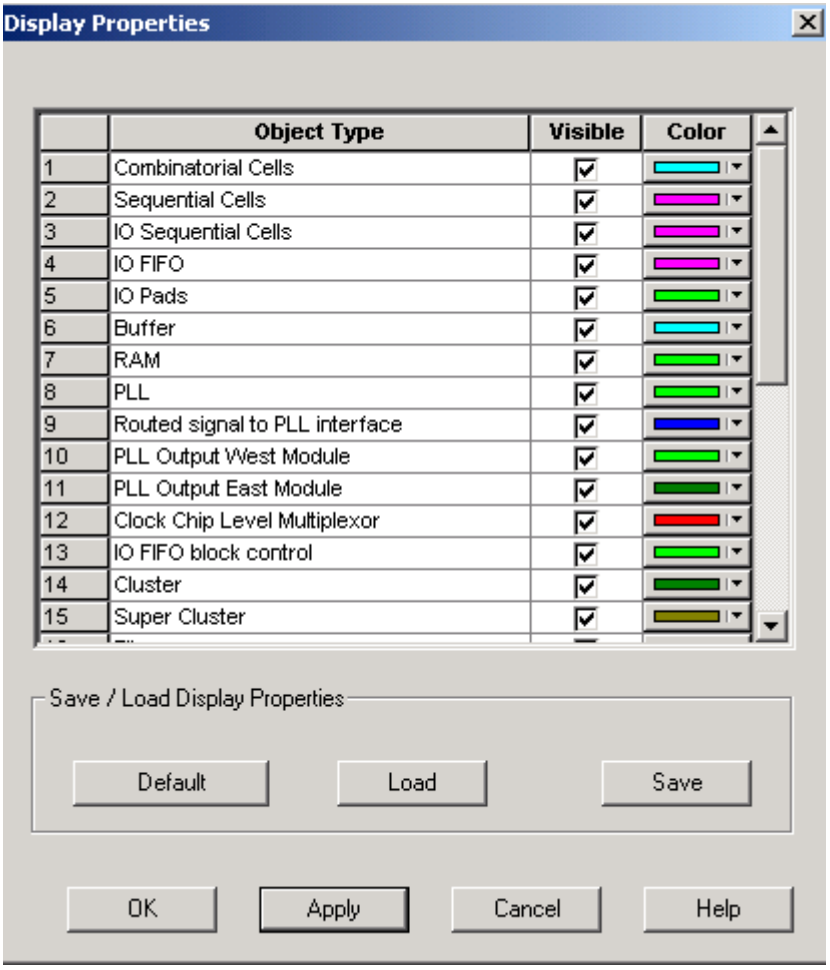
3. Enter a patten in the Pattern text box and click **Find**. All macros connected to the net appear.
4. Select the macro or macros in the left list box and click **Assign**.

Displaying Resources

To control what architectural features are displayed in ChipPlanner, use the Display Properties dialog box. For detailed information about supported architectural features, see the data sheet.

To set display properties:

1. From the **View** menu, click **Display Settings**.



Display Properties Dialog Box

All the architectural features that can be displayed appear in the Display Properties dialog box.

2. To make an object visible, select the Visible checkbox.
3. To change the color used to display the object, click the color bar and select another color.
4. To save or open previously saved Display Properties:

- Click **Save** to save your display properties to a file.
- Click **Load** to open a saved display properties file.
- Click **Default** to load the default display properties.

5. Click **Apply** to see your changes.
6. Click **OK** to dismiss the dialog box.

Ratsnest

The ratsnest view displays net connectivity between placed logic macros by connecting lines from the output pins to all input pins. Use the ratsnest to understand how logic macros are connected to each other. The ratsnest view is activated by default, showing all input and output nets for the selected macro.

Turn the Ratsnest view on or off by clicking the Ratsnest toolbar button.

Route view

The route view displays a representation of the actual routes used to connect placed macros. This feature helps show the general location of routing segments used by the design.

To activate the route view in ChipPlanner:

1. Complete Layout. To display routes, Layout must be completed before running ChipPlanner.
2. From the **Nets** menu, click **Show Routes** or click the Show Routes toolbar button.

3. Select the placed macro in the ChipPlanner window or Physical Hierarchy tab. Select multiple macros by holding down the CTRL key.

Clusters and SuperClusters

A cluster is a group of logic elements. The type of elements that make up the cluster is determined by the device type.

A super cluster is at least 2 clusters (SX) or 2 clusters and a buffer (Axcelerator). Modules in a cluster can be connected by fast or direct connects.

Use these areas as guides to ensure that the nets are fast/direct connect for implementation. Nets that connect within a rectangle can be implemented as fast or direct connects, depending on availability. For details about fast connects and direct connects, please see the Actel FPGA Databook.

Note: This feature is only available for the SX, SX-A, eX, and Axcelerator families.
To view clusters or super clusters in ChipPlanner:

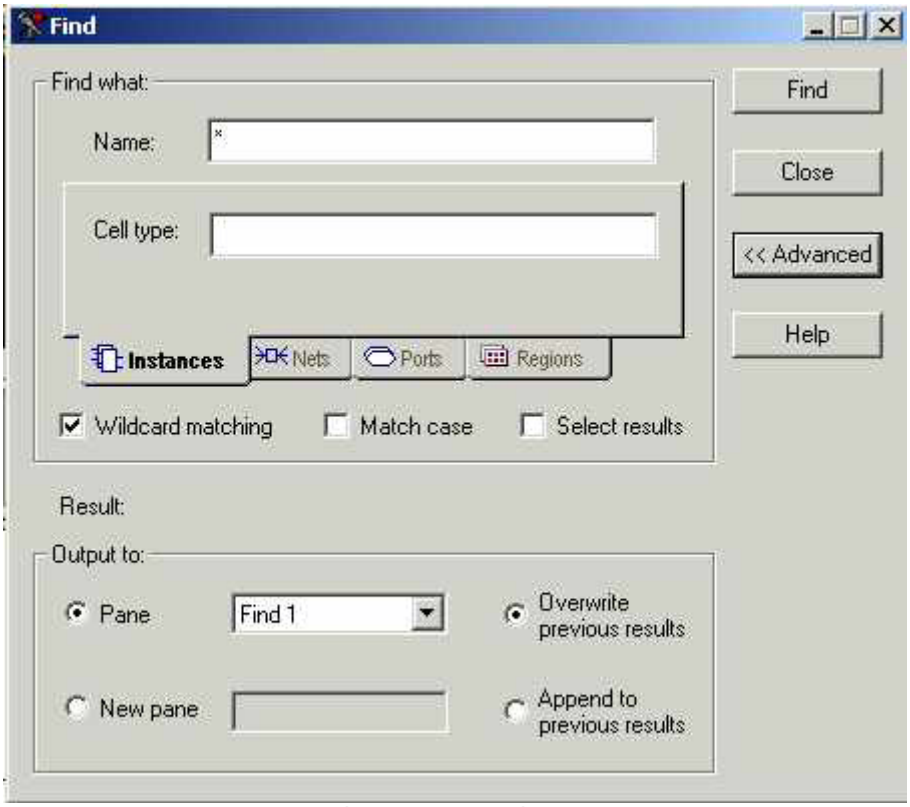
1. From the **View** menu, click **Display Settings**. The Display Properties dialog box appears.
2. Locate cluster or super cluster and select the Visible check box. Click the color bar to change the display color.
3. Click **OK**.

Finding objects

Use the Find feature in the MultiView Navigator to locate instances, nets, ports, and regions. You can use the Find feature when using any tool that opens in the MultiView Navigator interface.

To find instances:

1. From the **Edit** menu, click **Find**. The find dialog appears.
2. Click the **Instances** tab.



Find Instances Dialog Box

3. To search by name, type the name and Cell Type in the **Name** and **Cell Type** fields. When searching for instances, Instance Name or Cell Type can be blank, but not both.

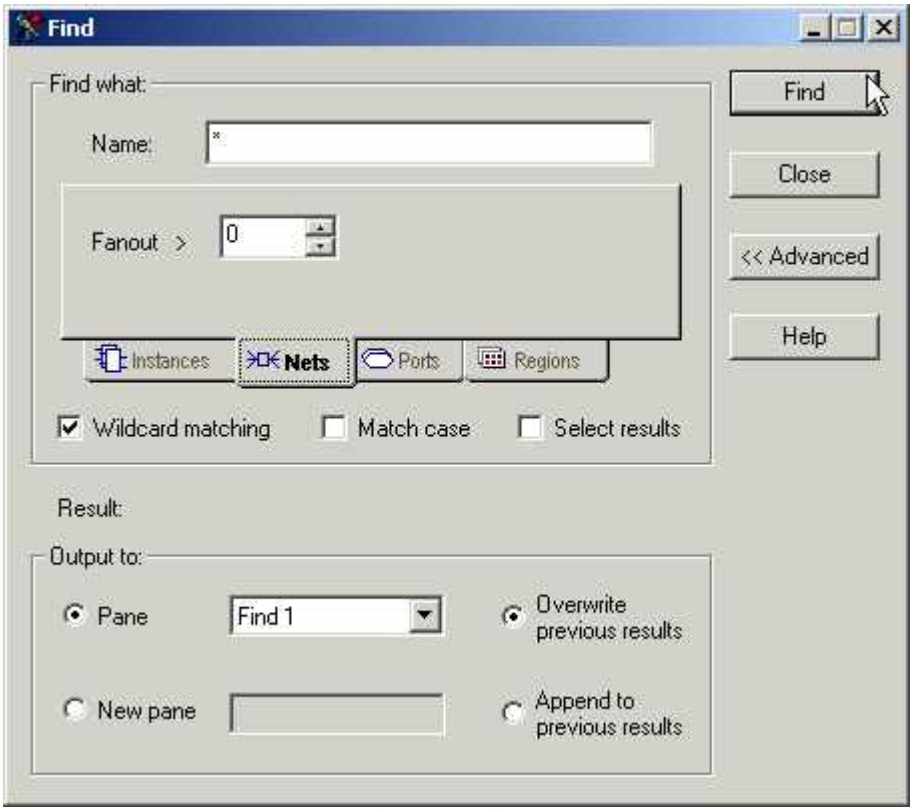
These fields accept regular expressions. Wildcards in regular expression include:

- ? matches any single character
- * matches any string
- [ ] matches any single character among those listed between brackets
- [A-Z] matches any single character in range A-Z
- [Z-A] matches any single character in range A-Z
- / is the level-bordering symbol. "A/B" designates "object B, which is part of instance A". Note that the level-bordering symbol cannot be put between brackets in a regular expression.

4. Select **Wildcards** if you want to search using wildcards.
5. Select **Match case** if you want the search to only return items with the exact characters specified.
6. Click **Advance** to specify how you want your results displayed. Specify or create a new pane in the log window to display your results. If you use an existing pane, you can choose to overwrite your previous results or append the new results.
7. Click **Find**. The located instances, if any, appear in the Find pane in the log window.

To find a net:

1. From the **Edit** menu, click **Find**. The find dialog appears.
2. Click the **Nets** tab.



Find Nets Dialog Box

2. Type the **name** of the net. This field accepts regular expressions. Wildcards in regular expression include:

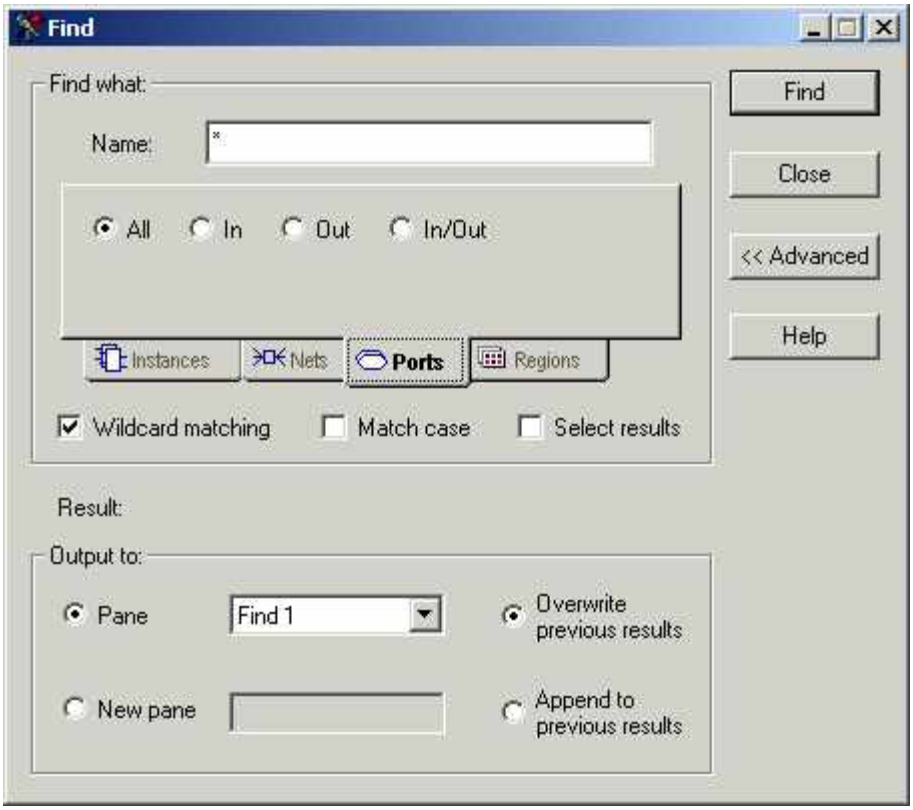
- ? matches any single character
- * matches any string
- [ ] matches any single character among those listed between brackets
- [A-Z] matches any single character in range A-Z
- [Z-A] matches any single character in range A-Z

- / is the level-bordering symbol. "A/B" designates "object B, which is part of instance A". Note that the level-bordering symbol cannot be put between brackets in a regular expression.

3. Select **Wildcards** if you want to search using wildcards.
4. Select **Match case** if you want the search to only return items with the exact characters specified.
5. Click **Advance** to specify how you want your results displayed. Specify or create a new pane in the log window to display your results. If you use an existing pane, you can choose to overwrite your previous results or append the new results.
6. Click **Find**. The located nets, if any, appear in the Find pane in the log window.

To find ports:

1. From the **Edit** menu, click **Find**. The find dialog appears.
2. Click the **Ports** tab.

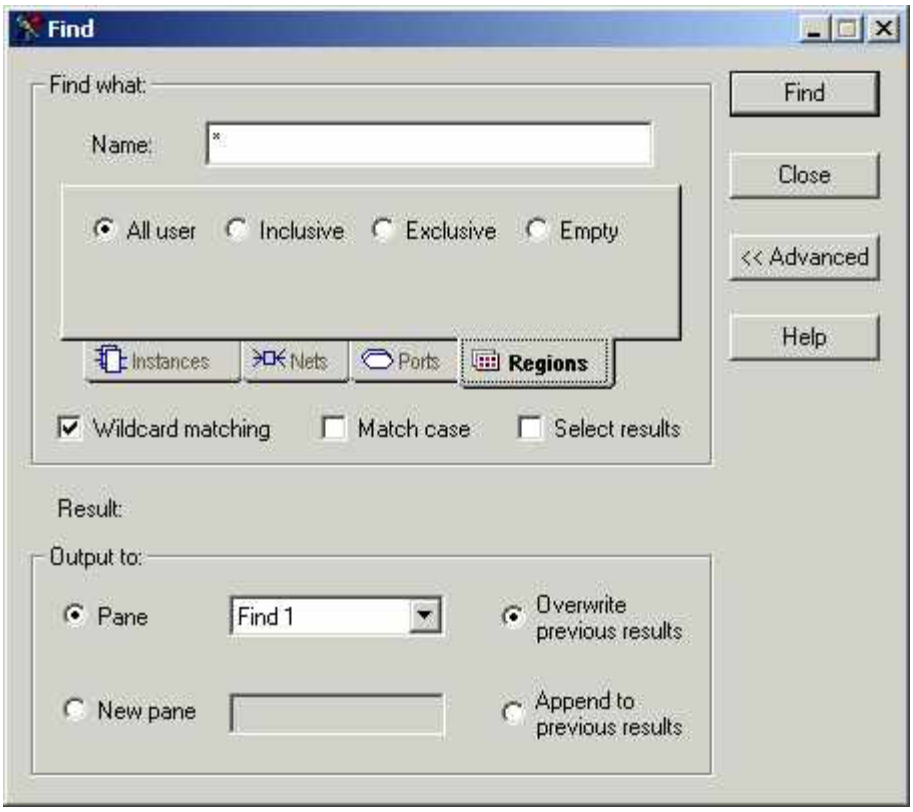


Find Ports Dialog Box

3. To search by name, type the **Name** of the port to be located. These fields accept regular expressions. Wildcards in regular expression include:
    - ? matches any single character
    - matches any string
    - [ ] matches any single character among those listed between brackets
    - [A-Z] matches any single character in range A-Z
    - [Z-A] matches any single character in range A-Z
    - / is the level-bordering symbol. "A/B" designates "object B, which is part of instance A". Note that the level-bordering symbol cannot be put between brackets in a regular expression.
4. To find a port by type, select **All**, **In**, **Out**, or **In/Out.**
5. Select **Wildcards** if you want to search using wildcards.
6. Select **Match case** if you want the search to only return items with the exact characters specified.
7. Click **Advance** to specify how you want your results displayed. Specify or create a new pane in the log window to display your results. If you use an existing pane, you can choose to overwrite your previous results or append the new results.
8. Click **Find**. The located ports, if any, appear in the Find pane in the log window.

To find regions:

1. From the **Edit** menu, click **Find**. The Find dialog box appears.
2. Click **Regions**.



Find Regions Dialog Box

3. To search by name, type the **Name** of the region you want to find. These fields accept regular expressions. Wildcards in regular expression include:

- ? matches any single character
- * matches any string
- [ ] matches any single character among those listed between brackets
- [A-Z] matches any single character in range A-Z
- [Z-A] matches any single character in range A-Z
- / is the level-bordering symbol. "A/B" designates "object B, which is part of instance A". Note that the level-bordering symbol cannot be put between brackets in a regular expression.

4. To search by type of region, select **All User**, **Inclusive**, **Exclusive**, and **Empty**.

About I/O Banks

For devices that support multiple I/O standards, I/Os are grouped onto I/O banks around the chip.

The Axcelerator Family has 8 I/O banks that surround the chip, two per-side, numbering 0-7. The I/O banks are color coded for quick identification. (Colors can be changed using the Color Manager.)

Each I/O bank has a common:

- VCCI, the supply voltage for its I/Os
- VREF, the reference voltage bus (for voltage-referenced I/O standards)

Only one VREF value can be assigned to each I/O bank. Only I/Os compatible with both the same VCCI and VREF standards can be assigned to the same bank.

Assigning technologies to I/O banks

To assign technologies to banks:

1. Select an I/O bank.
2. From the **Tools** menu, click **I/O Bank Settings**.
3. In the I/O Bank Properties dialog box, select your options and click **Apply**. The I/O bank is assigned the selected standards. Any I/O of the selected types can now be assigned to that I/O bank. Any previously assigned I/Os in the bank that are no longer compatible with the standards applied are removed.
4. If VREF pins can be assigned, the Assign VREF Pins button will highlight.

5. Assign I/O standards to other banks by selecting the banks from the list and assigning standards. Any banks not assigned I/O standards use the default standard selected in the Device Selection Wizard.
6. Click **OK**. Using PinEditor, proceed to assign I/Os with the same standards to the appropriate banks.

I/O Bank options

When assigning technologies to your I/O banks, use the I/O Bank Settings dialog box.

Options include:

Select Technologies

Selecting a standard selects all compatible standards and grays out incompatible ones. For example, selecting LVTTL also selects PCI, PCIX, and LVPECL, since they all have the same VCCI. Further selecting GTL (3.3V) disables SSTL3 as an option because the VREFs of the two are not the same.

Assign VREF Pins

After you have selected your technology, click Apply. If VREF pins are required, this button becomes activated. Click to assign VREF pins. You must assign VREF pins at least once.

Click More Attributes to set the following:

Low Power Mode (Optional)

Select Enable Input Buffers or Enable Output Buffers. These are not required. This feature is not supported in the RTAX-S family.

Input Delay

Drag the slider bar to your desired delay. The delay is bank specific. Drag the meter to your desired delay index. The delay code and typical value appear. Click **View All Delays** to see all the delay values (Best, Worst, Typical, Rise-Rise, Fall-Fall) for the input delay selected. A

technology must be selected in order to see the input delays. Click **OK** to dismiss the View All Delays dialog box. This feature is not supported in the RTAX-S family.

Assigning VREF pins

Voltage referenced I/O inputs require an input referenced voltage (VREF).

To assign VREF pins:

1. From the **Tools** menu, click **I/O Bank Settings**.
2. Specify the supported technologies for the I/O bank and click **Apply**.
3. If VREF pins can be assigned, the Assign VREF Pins button activates.
4. Click **Assign VREF Pins**. The Assign VREF Pins dialog box appear
5. Check the VREF box next to the pin number and click OK. Click the Reset to Defaults button to revert to Actel recommended defaults.
6. Click **OK** to dismiss the Assign Vref Pins dialog box dialog box.
7. Click **OK** to dismiss the **I/O Bank Properties** dialog box.

Specifying I/O bank voltage

You can directly specify voltages for each I/O bank by doing one of the following:

- Using the I/O Bank Properties dialog box
- Placing an I/O of a particular technology in an I/O bank that has not been assigned a voltage
- Using the command set_iobank in a PDC File

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