Actel® Tools

PinEdit User's Guide

R1-2003

Windows® & UNIX® Environments

Actel® Corporation, Sunnyvale, CA 94086

Part Number: 5029119-4

Release: December 2002

Trademarks

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Introduction

The PinEdit tool provides a graphical interface that allows you to customize I/O placement and attributes.

For non Axcelerator families, Actel recommends that you let Designer automatically assign I/O locations during layout. Layout is designed to place the I/Os for optimum routability and performance.

When targeting the Axcelerator family, and individual I/O bank configuration is necessary, PinEdit must be used to assign I/O standards to each bank *before running Layout*. All banks not assigned a specific I/O standard will inherit the default I/O standard selected in the Device Selection Wizard.

You can assign I/O locations automatically in your design schematic or by importing one of the following:

- PIN file
- Gatefield Constraint File (.gcf) (ProASIC and ProASIC PLUS families only)
- Physical Design Constraint (.pdf) (Axcelerator family only)

Note: Refer to documentation included with your CAE tools for information about assigning I/O signal placement in a schematic or using a pin file. Refer to the *Designer User Guide* for information about PDC files.

Pin Edit offers you a manual option for design optimization. Use PinEdit to:

- assign I/O macros
- view and print pin assignments
- fix pin assignments automatically assigned by Designer to maintain the pin locations during layout
- edit I/O attributes, such as I/O standards, specifications, slew, and capacitance
- assign I/O standards to banks, for devices that utilize I/O banks to support multiple I/O standards
- assign VREF pins, if an assigned I/O standard requires an input reference voltage

Document Organization

This guide provides detailed cross-platform information about PinEdit, including step-by-step instructions for using PinEdit on Windows and UNIX workstations. Any differences between platform procedures and commands are noted in the text.

The PinEdit User's Guide contains the following chapters:

Chapter 1- Getting Started with PinEdit contains details about PinEdit's interface, toolbars, and menu commands.

Chapter 2- Using PinEdit contains instructions on how to use PinEdit to assign I/O attributes and how to view, edit, and fix pin locations.

Appendix A - Product Support provides information about contacting Actel for customer and technical support.

Appendix B - Glossary provides definitions for key terms used in this guide.

Document Assumptions

This document assumes you have a working knowledge of your operating system and its conventions, including standard menus and commands. It also assumes you know how to use a mouse, and how to open, save, and close files. For help with any of these techniques, see the documentation that came with your computer.

This document assumes you are familiar with the FPGA architectures and design flows, as well as the Designer software.

Your Comments

Actel Corporation strives to produce the highest quality online help and printed documentation. We want to help you learn about our products and get your work done quickly. We welcome your feedback about this guide and our online help. Please send your comments to **docs@actel.com**.

Actel Manuals

Libero includes printed and online manuals. The online manuals are in PDF format and available from Libero's Start Menu and on the CD-ROM.

From the Start menu choose:

- Programs > Libero 2.2 > Libero 2.2 Documentation.
- Programs > Designer Series > R1-2002 Documentation

From the CD, insert your CD-ROM and click *Documentation* from the main screen, or look on the CD-ROM in the "/doc" directory. These manuals are also installed onto your system when you install the Libero software. To view the online manuals, you must install Adobe® Acrobat Reader® from the CD-ROM.

Libero includes the following manuals, which provide additional information on designing Actel FPGAs:

Libero User's Guide. This manual contains information about using Libero, Actel's Integrated Design Environment. Details about using ViewDraw for Actel, WaveFormer Lite, Synplicity, and ModelSim are provided.

Getting Started User's Guide. This manual contains information for using the Designer Series Development System software to create designs for, and program, Actel devices.

Designer User's Guide. This manual provides an introduction to the Designer series software as well as an explanation of its tools and features.

PinEdit User's Guide. This guide provides a detailed description of the PinEdit tool in Designer. It includes cross-platform explanations of all the PinEdit features.

ChipEdit User's Guide. This guide provides a detailed description of the ChipEdit tool in Designer. It includes a detailed explanation of the ChipEdit functionality.

Timer User's Guide. This guide provides a detailed description of the Timer tool in Designer. It includes a detailed explanation of the Timer functionality.

SmartPower User's Guide. This guide provides a detailed description of using the SmartPower tool to perform power analysis.

Netlist Viewer User's Guide. This guide provides a detailed description of the Netlist Viewer. Information on using the Netlist Viewer with Timer and ChipEdit to debug your netlist is provided.

A Guide to ACTgen Macros. This Guide provides descriptions of macros that can be generated using the Actel ACTgen Macro Builder software.

Actel HDL Coding Style Guide. This guide provides preferred coding styles for the Actel architecture and information about optimizing your HDL code for Actel devices.

Silicon Expert User's Guide. This guide contains information to assist designers in the use of Actel's Silicon Expert tool.

Cadence® Interface Guide. This guide contains information to assist designers in the design of Actel devices using Cadence CAE software and the Designer Series software.

Mentor Graphics® Interface Guide. This guide contains information to assist designers in the design of Actel devices using Mentor Graphics CAE software and the Designer Series software.

Synopsys®Synthesis Methodology Guide. This guide contains preferred HDL coding styles and information to assist designers in the design of Actel devices using Synopsys CAE software and the Designer Series software.

Synplicity Synthesis Methodology Guide. This guide contains information about using the Synplicity Synthesis tools with Actel Designer Series software to create designs for Actel devices.

Innoveda® eProduct Designer Interface Guide (Windows). This guide contains information to assist designers in the design of Actel devices using eProduct Designer CAE software and the Designer Series software.

VHDL Vital Simulation Guide. This guide contains information to assist designers in simulating Actel designs using a Vital compliant VHDL simulator.

Verilog Simulation Guide. This guide contains information to assist designers in simulating Actel designs using a Verilog simulator.

Activator and APS Programming System Installation and User's Guide. This guide contains information about how to program and debug Actel devices, including information about using the Silicon Explorer diagnostic tool for system verification.

Silicon Sculptor User's Guide. This guide contains information about how to program Actel devices using the Silicon Sculptor software and device programmer.

Flash Pro User's Guide. This guide contains information about how to program Actel ProASIC and ProASIC PLUS devices using the Flash Pro software and device programmer.

Silicon Explorer II. This guide contains information about connecting the Silicon Explorer diagnostic tool and using it to perform system verification.

Macro Library Guide. This guide provides descriptions of Actel library elements for Actel device families. Symbols, truth tables, and module count are included for all macros.

ProASIC PLUS Macro Library Guide. This guide provides descriptions of Actel library elements for Actel ProASIC and ProASICPLUS device families. Symbols, truth tables, and tile usage are included for all macros.

WaveFormer Lite Guide. This guide contains information on using WaveFormer Lite to generate VHDL and Verilog stimulus based test benches for the Actel design software.

ViewDraw User's Guide. This guide contains information about using ViewDraw.

ModelSim Bookshelf. This bookshelf contains the ModelSim User's Guide, Command Reference, and Tutorial.

Online Help

Libero comes with online help. Online help specific to each Actel software tool is available for Designer, ACTgen, Silicon Expert, Silicon Explorer II, Silicon Sculptor, and APSW.

1

Getting Started with PinEdit

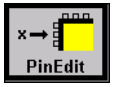
This chapter contains details about PinEdit's user interface and commands. For information on using PinEdit to customize I/O macro assignments and attributes, please refer to "Using PinEdit" on page 27.

Starting PinEdit

PinEdit is not a stand-alone tool; you can only start it from Designer. There are three ways to invoke PinEdit from Designer:

- From the Tools menu, click *PinEdit*
- Click PinEdit in Designer's toolbar

- Click PinEdit in Designer's Design Flow Window.



PinEdit opens in a separate window displaying pins, I/O macros, and I/O attributes in your design, as illustrated in Figure 1-1 on page 16.

Note: PinEdit requires a compiled netlist. Therefore, you can only invoke PinEdit after you have opened an existing design (an *.adb) in a compiled state, or after you have compiled your netlist in Designer. If you invoke PinEdit before compiling your netlist, Designer guides you through the compile process before opening PinEdit.

PinEdit

PinEdit's workspace, as illustrated in Figure 1-1 and Figure 1-2, consists of specialized windows and tools that help you customize pin placements and attributes.

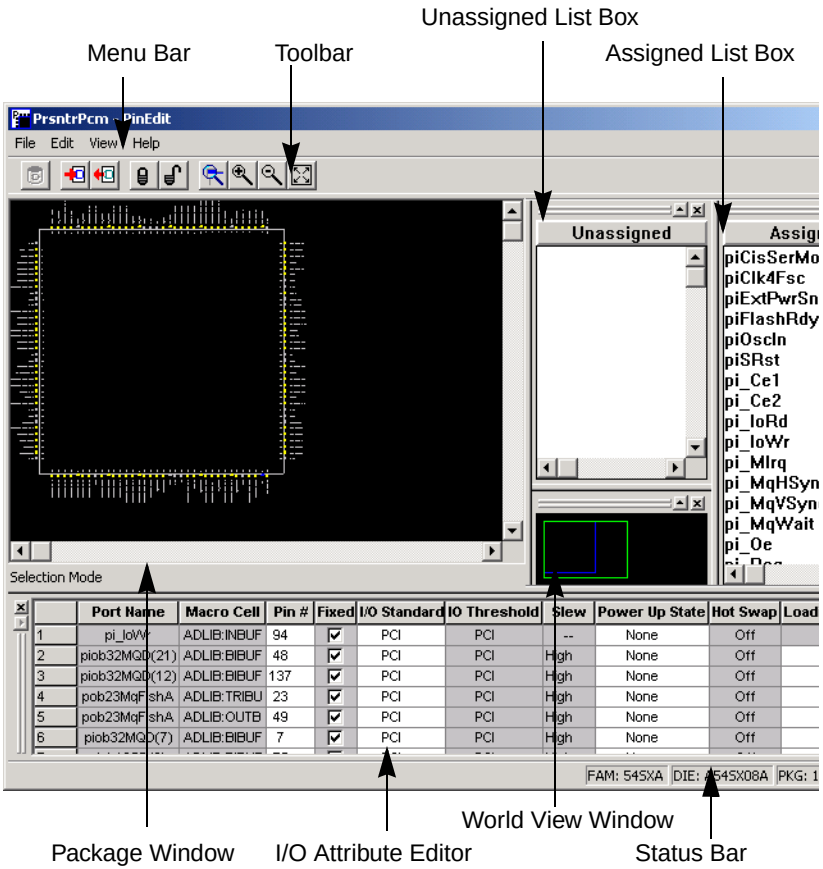


Figure 1-1. PinEdit - SX Design

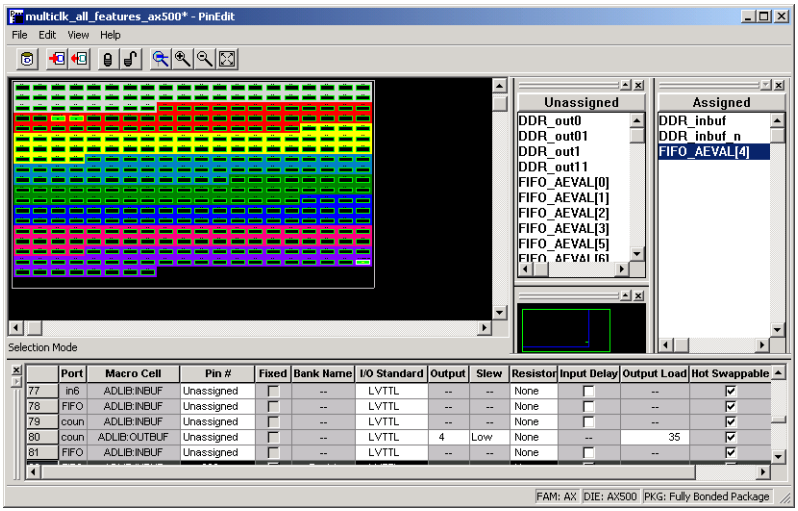


Figure 1-2. PinEdit, Axcelerator Design

PinEdit includes a Package window, World View window, Assigned and Unassigned list box windows, and an I/O Attribute Editor window. These windows are highly integrated; anything selected in one is selected or highlighted in all. Commands are accessible from the command menu bar and frequently used commands are on the toolbar.

All the windows and bars are independently sizeable, dockable and closable. To redock or refloat a window, double-click the window's title bar. On UNIX systems, floating windows are not sizeable once undocked and the I/O Editor does not float.

Package Window

PinEdit's Package window displays pins, I/O macro assignments, and I/O Banks (Axcelerator family only).

The Package window is integrated with PinEdit windows and list boxes. If you select an assigned pin in the Package window, the pin location is highlighted in

the World View window and the I/O macro name is selected in the Assigned list box and the I/O Attribute Editor.

The Package Window displays detailed information about each pin, including:

- pin number
- special pin properties, such as JTAG, clock, ground, or power
- assigned I/O macro name, if any
- pin type, represented by color

PinEdit Colors and Symbols

Pin and I/O macro assignments are color coded in the Package window. Table 1-1 describes the colors used in the Package window.

Table 1-1. PinEdit: Colors and Symbols

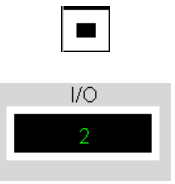
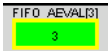
Color	Definition
White border 	Selected empty pin(s).
Green with black center 	Regular, unassigned pin.
Blue with black center 	A special, unassigned pin. A pin with a grey or yellow border and a blue center denotes a special, assigned pin. Special pins are pins that have some additional meaning to them. For example, pins used for JTAG are blue. When unassigned, special pins have additional descriptive text next to the pin number.

Table 1-1. PinEdit: Colors and Symbols

Color	Definition
Grey with red center 	Reserved pin. You use this pin for some specific purpose on the package and you cannot assign it an I/O macro. Examples of such pins are ground and power.
Grey with green center 	Assigned, unfixed pin.
Yellow with green center  	Fixed assignment.
Grey/black	A pin with a grey border and a black center denotes a pin that is not connected. You cannot use these pins and they have no meaning.

Color Manager

Use the Color Manager to customize the colors used to display the package in ChipEdit and PinEdit. The Color Manager specifies the display colors for I/O banks, I/O FIFO Blocks, RAM tiles, Core tiles, clusters, super clusters, and nets.

To customize the colors in the Package window:

1. **Click *Color Manager* from the View menu.** The color manager dialog box is displayed,as shown in Figure 1-3.

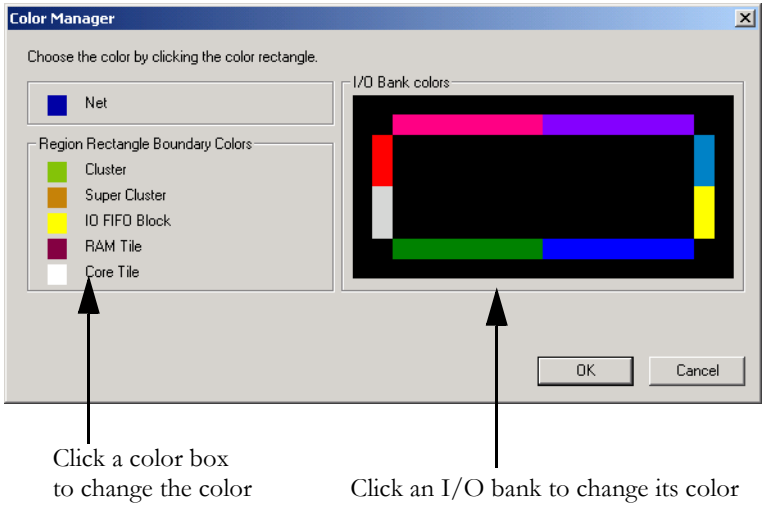


Figure 1-3. Color Manager

Note: The region rectangle boundaries and nets are not visible in PinEdit.

2. **Click the color box in front of the item you wish to customize, or click the I/O bank you wish to change.** The color pallet is displayed, as shown in Figure 1-4.

Figure 1-4. Color Palette

3. **Select a color and click *OK*.** The new color will appear in the Color Manager dialog box.
4. **After you are done customizing your colors using the Color Manger dialog box, click *OK*.**

World View Window

The World View window's default location is under the Assigned list box. Use the World View window to control which portion of the package is displayed in the Package window. The blue rectangle (known as the Package rectangle) represents the package. The green rectangle (known as the Viewing rectangle) represents the currently displayed area in the Package window.

To display another part of the package, use the left mouse button to drag the Viewing rectangle to the area on the Package rectangle you would like to display. To specify a new display area, use the right mouse button to stroke out a new Viewing rectangle on the Package rectangle.

Assigned and Unassigned List Boxes

The Assigned and Unassigned list boxes display assigned or unassigned I/O macros in the design. By default, all assigned I/O macros are displayed in the Assigned list box and all unassigned I/O macros are displayed in the Unassigned list box. Use the Configure List Boxes dialog box, as shown in Figure 1-5 on page 22, to change the default behavior of the Assigned and Unassigned list boxes.

Configuring List Boxes

Use the Configure List Box dialog box to customize what is displayed in the Assigned and Unassigned list boxes. The Configure List Box dialog box is displayed when you choose *Configure List Boxes* from the View menu, or by right-clicking in the Assigned or Unassigned list box and selecting *Configure List Boxes*.

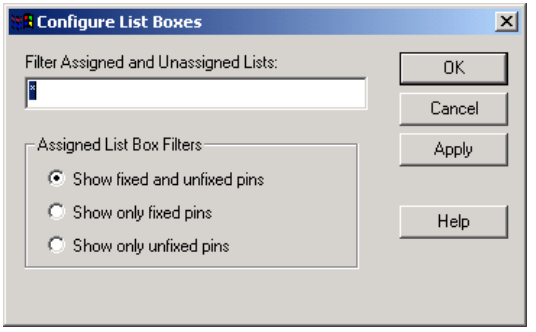


Figure 1-5. Configure List Boxes Dialog Box

- **Filter Assigned and Unassigned Lists**: Entering a specific pin name in this field filters out all other pins in the Assigned and Unassigned List Boxes. Use the * wildcard to filter for groups.
- **Show fixed and unfixed pins**: Selecting this causes all fixed and unfixed pins to be displayed in the Assigned list box.
- **Show only fixed pins**: Selecting this filters out all unfixed pins from the Assigned list box.
- **Show only unfixed pins**: Selecting this filters out all fixed pins from the Assigned list box.

Click *Apply* to invoke changes. When satisfied, click *OK*.

I/O Attribute Editor

The default location of the I/O Attribute Editor is below the Package and World View windows. The I/O Attribute Editor lists all assigned and unassigned I/O macros and their attributes in a spreadsheet format. Use the I/O Attribute Editor to view, sort, select, and edit these I/O attributes. Double-click a column heading to sort by that attribute. If you select a macro in the list boxes, the I/O attribute editor scrolls to highlight the selected macro. For information on using the I/O Attribute Editor, refer to "I/O Attribute Editor" on page 23.

Toolbar

The PinEdit toolbar contains commands for performing common PinEdit operations on your designs. Click a button in the toolbar to access a command.

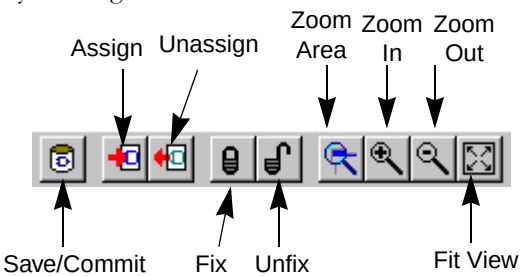


Figure 1-6. PinEdit Toolbar

If you position the mouse pointer over a toolbar button, a short description called a tooltip is provided. A longer description appears in the status bar at the bottom of the main window.

PinEdit's toolbar is floatable. This means you can drag it to any edge of the window, or by dragging it from any edge, you can leave it floating over your work. Drag the toolbar from its separator bar to avoid clicking toolbar buttons by mistake.

PinEdit Menu Commands

The PC and UNIX versions of PinEdit have the same menus. However, some dialog boxes may look slightly different due to the different windowing environments. The functionality is the same, though the locations of the fields and buttons on the dialog boxes may vary. Field names may also vary between platforms.

File Menu

Commit: Commits Pin Assignments to Designer.

Print: Prints Pin Assignments.

Close: Closes the PinEdit window.

Edit Menu

Copy: Copies selection to the clipboard.

Assign: Assigns the selected I/O macro to the next selected pin.

Unassign: Unassigns the selected I/O macro.

Fix: Fixes the selected I/O macro.

Unfix: Unfixes the selected I/O macro.

Select All: Selects all assigned I/O macros.

Configure I/O Banks: Opens the Configure I/O Banks dialog box, where you can assign compatible I/O standards to banks. (Axcelerator family only)

View Menu

Zoom Area: Enlarges a user-defined rectangular region of the design.

Zoom In: Reduces the displayed area of the design.

Zoom Out: Enlarges the displayed area of the design.

Fit in Window: Fits the entire design view in the Package window.

Redraw: Refreshes the package view in the Package window.

Configure List Boxes: Filters which pins to display in the list boxes.

Color Manager: Customizes colors displayed in Package Window.

I/O Banks: View or hide the I/O banks.

Toolbar: View or hide the toolbar.

Assigned List Box: View or hide the Assigned list box.

Unassigned List Box: View or hide the Unassigned list box.

World View: View or hide the World View window.

I/O Attribute Editor: View or hide the I/O Attribute Editor.

Status Bar: View or hide the Status Bar.

Help Menu

Help Topics: Opens the online Help.

Reference Manual: Opens an index of help topics.

Extended Error Messages: Opens a dialog box with more information on error messages. See Figure 1-7 on page 26.

Status Bar

Family, die, and package information appears in the right corner of the status bar. In addition, the status bar displays information on commands, pins, and error messages.

- Hold your mouse over a pin in the Package window to see the pin number, instance name, macro cell, and fixed or unfixed status in the Status Bar.
- If you hold your mouse over a toolbar icon or a menu command, a short description of the command function appears in the Status Bar.
- Error messages in the Status Bar provide details about invalid placement attempts. Choose *Extended Error Messages* from the Help menu to view more

information about the error message (Figure 1-7).

Figure 1-7. Extended Error Messages

2

Using PinEdit

Use PinEdit to customize I/O macro assignments and attributes. For a complete description of PinEdit's interface and menu commands, see "Getting Started with PinEdit" on page 15.

Pin Assignments

Use PinEdit to make and edit I/O macro pin assignments. Edits made in PinEdit are permanent, as long as they are fixed and committed (see "Fixing and Committing Pin Assignments" on page 42).

To assign an I/O macro to a pin:

1. **Select the macro name in the Unassigned list box.** The macro is simultaneously selected in the I/O Attribute Editor.
2. **Assign the macro to a pin.** Assign the selected macro to a pin location using any one of these methods:
   - **Drag and Drop:** Drag the selected macro name from the Unassigned list box to the pin location in the Package Window. Valid pin locations are high-lighted in the Package Window.
   - **Menu Commands:** In the Edit menu, choose *Assign* to invoke the Assign mode. Then, select the pin location in the Package Window.
   - **Toolbar Commands:** Click the *Assign* icon to invoke the Assign mode. Select the pin location in the Package window.
   - **I/O Attribute Editor:** If you know the specific pin location, enter the pin assignment in the *Pin#* cell or select a valid placement from the drop-down menu.

If the location is a valid one, the macro is assigned and automatically fixed. (For details about fixing and unfixing, see "Fixing and Committing Pin Assignments" on page 42.) The status bar displays information about invalid assignments. Choose *Extended Error Messages* from the Help menu for more information about specific error messages.

Note: If you assign a macro to a pin that has already been assigned a macro, the previously assigned macro becomes unassigned even if its placement has been fixed.

Assigning Multiple I/O Macros

To make multiple pin assignments, as in the case of a bus, it is easier to assign the I/O macros as a group.

To assign multiple I/O macros:

1. **Select I/O macros.** Hold down the CTRL or SHIFT key and select multiple I/O macros in the order you want them assigned.
2. **Activate the Assign mode.** In the Edit menu, click *Assign*.
3. **Assign Macros.** Select pin assignments in the Package window. The I/O macros will be assigned in the order selected.

Assigning I/O Macro Groups

In some cases, you do not need to select multiple I/O macros to create a group. Some macros are grouped into macro groups or pairs, as in the case of LVDS or LVPECL pairs. You do not need to individually select and assign macros in groups such as these; all I/Os in the group are selected and assigned with a single placement.

To assign an I/O macro group:

1. **Select the I/O macro group in the unassigned column.**
2. **Drag and drop the block onto a pin module. PinEdit assigns all the I/O modules in the group to suitable legal location.**

Unassigning I/O Macros

Unassign an I/O macro from a fixed placement when its fixed position is no longer required. Unassigned macros are automatically placed in optimum locations during layout.

To unassign a macro:

1. **Select the I/O macro in the Assigned box.**
2. **Unassign the I/O macro.** Unassign the selected macro using any one of the following methods:
   - **Keyboard:** Press the DELETE key.
   - **Drag and Drop:** Drag the selected macro name from the Assigned list box to the Unassigned list box.

- **Menu Commands:** In the Edit menu, click *Unassign*.
- **Toolbar:** Click the *Unassign* icon.
- **I/O Attribute Editor:** Select *Unassign* in the Pin # cell.

The macro is unassigned.

To unassign multiple macros:

1. **Select macros to unassign.** In the Assigned list box, hold down the CTRL or SHIFT key and select multiple I/O macros with your mouse. Alternatively, select all I/O macros by choosing *Select All* from the Edit menu.
2. **Unassign the macros.** In the Edit menu, click *Unassign*. All selected I/O macros are unassigned.

Editing I/O Macro Pin Assignments

There are multiple ways to edit macro pin assignments.

To edit I/O macro pin assignments:

1. **Select the macro in the I/O Attribute Editor, the Package window, or the Assigned list box.**
2. **Edit the assignment using one of the following methods:**
   - In the I/O Attribute Editor, enter the new Pin Assignment in the Pin # cell. Type in the pin number or select a valid pin from the list. The Assigned and Unassigned list boxes are updated accordingly.
   - Drag and drop the selected macro in the Package window or, from the Assigned list box, to its new pin location in the Package window.

   If you assign a macro to a pin that has already been assigned a macro, the previously assigned macro becomes unassigned. Since PinEdit fixes all assigned macros, the reassignment unfixes the previous assignment.

   Note: In rare cases, you will not be able to move certain clock macros because the clock occupies two modules. The two modules are only visible in ChipEdit. Use ChipEdit to move these clock modules.

Printing Pin Assignments

PinEdit prints the package view, showing all package pins, special properties, and assigned I/O macros.

To print the package view:

1. **In the File menu, click *Print*.** The Printer dialog box is displayed.
2. **Select your printer options and click *OK*.**

For information on setting up a printer in UNIX, please refer to the Setting Up a Printer in UNIX appendix in the Designer User's Guide.

Generating Pin Reports

Designer generates pin reports from its main window. You can sort pin reports by name or number. The reports include the design name, family, die, and package.

To generate a pin report:

1. **Commit and Save your pin assignments.** In the File menu, click *Commit*.
2. **Return to the Designer main window and in the Tools menu, click *Reports*.** The Report Types dialog box appears.
3. **Select *Pin* from the drop-down report type menu and click *OK*.** The Pin Report Options dialog box appears.
4. **Select *Name or Number* from the List by drop-down menu.**
5. **Click *OK*.** The pin report appears in a new window.

I/O Banks

For devices that support multiple I/O standards, I/Os are grouped onto I/O banks around the chip. For the Axcelerator Family, there are 8 I/O banks surrounding the chip, two per-side, numbering 0-7. The I/O banks are color coded for quick identification. Colors can be customized using the Color Manager.

Each I/O bank has a common VCCI, the supply voltage for its I/Os. Each I/O bank also has a common reference voltage bus, VREF for the voltage-

referenced I/O standards. Only one VREF value can be assigned to each I/O bank. Only I/Os compatible with both the same VCCI and VREF standards can be assigned to the same bank. Table 2-1 shows compatible I/O standards.

Table 2-1. Legal I/O Usage Matrix

I/O Standard	LVTTL 3.3V	LVCMOS 2.5V	LVCMOS 1.8V	LVCMOS1.5V (JESD8-11)	3.3V PCI 3.3V, PCI-X	GTL + (3.3V)	GTL + (2.5V)	HSTL Class I (1.5V)	SSTL2 Class I & II (2.5V)	SSTL3 Class I & II (3.3V)	LVDS 2.5V ±5%	LVPECL (3.3V)
LVTTL 3.3V (V_{REF}=1.0V)	X				X	X						X
LVTTL 3.3V (V_{REF}=1.5V)	X				X					X		X
LVCMOS 2.5V (V_{REF}=1.0V)		X					X				X	
LVCMOS 2.5V (V_{REF}=1.25V)		X							X		X	
LVCMOS1.8V			X									
LVCMOS1.5V (V_{REF}=1.75V) (JESD8-11)				X				X				
PCI 3.3V, PCI-X (V_{REF}=1.0V)	X				X	X						X
PCI 3.3V, PCI-X (V_{REF}=1.5V)	X				X					X		X
GTL + (3.3V)	X				X	X						X
GTL + (2.5V)		X					X					
HSTL Class I				X				X				
SSTL2 Class I & II		X							X		X	
SSTL3 Class I & II	X				X					X		X
LVDS (V_{REF}=1.0V)		X					X				X	
LVDS (V_{REF}=1.25V)		X							X		X	
LVPECL (V_{REF}=1.0V)	X				X	X						X
LVPECL (V_{REF}=1.5V)	X				X					X		X

If standards can be used within a bank at the same time, you will find a “X” in the table. Examples:

a) LVTTL can be used together with itself, PCI3.3V, PCI-X, and GTL+ (3.3V), when VREF = 1.0V (GTL+ requirement).
b) LVTTL can be used together with itself, PCI3.3V, PCI-X, and SSTL3 Class I & II, when VREF = 1.5V (SSTL3 requirement).

To assign technologies to I/O banks:

1. **Select an I/O bank.**
2. **From the Edit menu, click Select *Configure I/O Banks*.** The Configure I/O Banks dialog box is displayed, as shown in Figure 2-1.

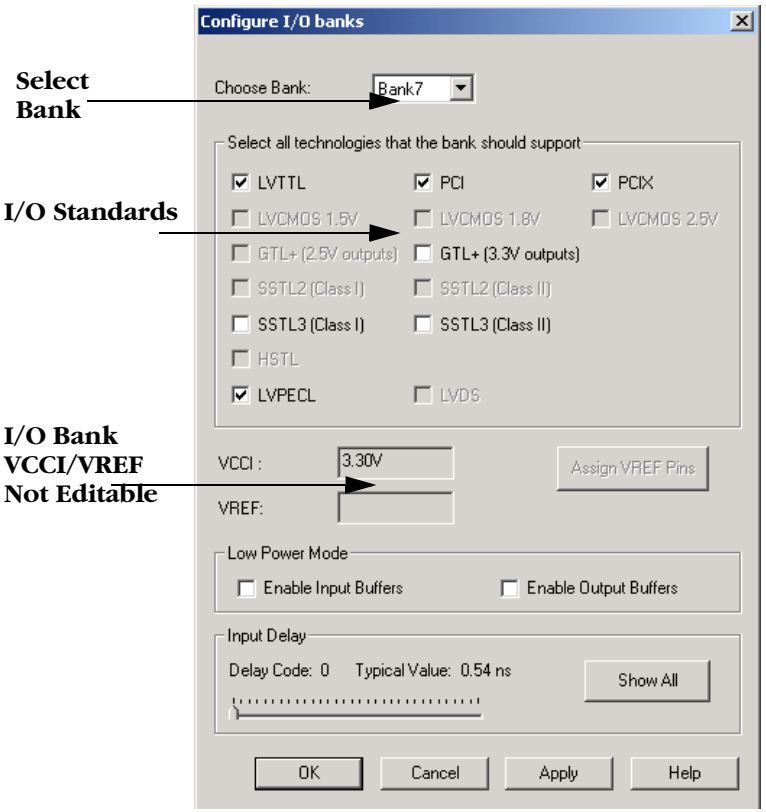


Figure 2-1. Configure I/O Banks Dialog Box

- **Select Technologies**: Selecting a standard selects all compatible standards and grays out incompatible ones. For example, checking LVTTL will check PCI, PCIX, and LVPECL, since they all have the same VCCI. Further selecting GTL (3.3V) disables SSTL3 as an option because the VREFs of the two are not the same.

- **Assign VREF Pins**: After you have selected your technology, click *Apply*. If VREF pins are required, this button becomes activated. Click to assign VREF pins. You must assign VREF pins at least once.
- **Low Power Mode (Optional)**: Select Enable Input Buffers or Enable Output Buffers. These are not required.
- **In Delay**: Drag the slider bar to your desired delay. The delay is bank specific. Drag the meter to your desired delay index. The delay code and typical value appear. Click *Show All* to see all the delay values (Best, Worst, Typical, Rise-Rise, Fall-Fall). A technology must be selected in order to see the input delays. Click *OK* to dismiss the Show All Delays dialog box.

3. **Make your selections and click *Apply*.** The I/O bank is assigned the selected standards. Any I/O of the selected types can now be assigned to that I/O bank. Any previously assigned I/Os in the bank that are no longer compatible with the standards applied are removed.

   If VREF pins can be assigned, the Assign VREF Pins button will highlight.

4. **Assign I/O standards to other banks by using the drop down list box to change banks.** Any banks not assigned I/O standards will use the default standard selected in the Device Selection Wizard.
5. **When you are done, click *OK*.** Proceed to assign I/Os with the same standards to the appropriate banks.

Assigning VREF Pins (Axcelerator family only)

Voltage referenced I/O inputs require an input referenced voltage (VREF).

To assign VREF pins:

1. **From the Edit menu, click *Configure I/O Banks*.**
2. **Specify the supported technologies for the I/O bank and click *OK*.**
3. **If VREF pins can be assigned, the Assign VREF Pins button activates.**

4. **Click the *Assign VREF Pins* button.** The Assign VREF Pins dialog box appears,as shown in Figure 2-2.

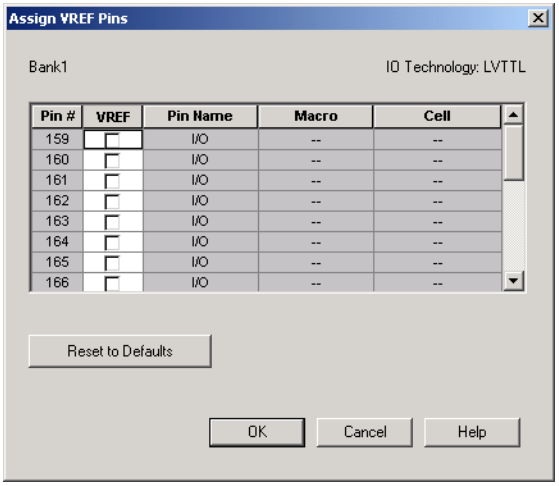


Figure 2-2. Assign VREF Pins Dialog Box

5. **To assign a VREF pin, check the VREF box next to the pin number and click *OK***. To revert to Designer's default settings, click the *Reset to Defaults* button.

6. **Click *OK* in the Configure I/O Banks dialog box.**

Specifying I/O Bank Voltages (Axcelerator family only)

You can directly specify voltages for each I/O bank by doing one of the following:

- Using the Configure I/O Banks dialog box
- Placing an I/O of a particular technology in an I/O bank that has not been assigned a voltage.
- Using the command 'set_iobank' in the Physical Design Constraints (PDC) File.

I/O Bank Voltage Assignments using the Configure I/O Banks Dialog Box

Bank voltages must be set before running Layout (place and route).

You can assign voltages to an I/O Bank using the Configure I/O Banks dialog box. When voltages are assigned, any previous I/O assignments not compatible are removed from the bank, appearing in the unassigned column.

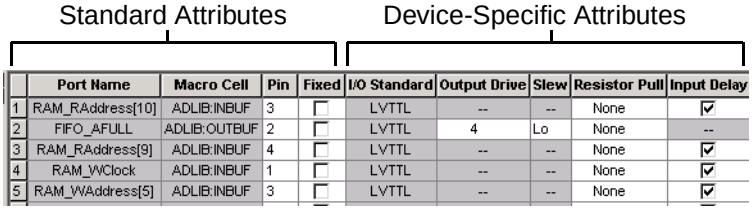
I/O Bank Voltage Assignments by Assigning I/O Macros

When a user assigns an I/O macro, the legality is checked according to the I/O Bank rules. It may sometimes happen that a pin occupying a VREF location will come in the way of placing a voltage referenced I/O. In this case, the I/O occupying the VREF will need to be unassigned first.

When a bank is without any voltage assignments, the I/O macros assigned to the bank will decide the voltages. These assignments will be undone if the macros in the bank become unassigned.

Setting I/O Attributes with the I/O Attribute Editor

The I/O Attribute Editor displays I/O attributes in a spreadsheet format. Use the I/O Attribute Editor to view, sort, select, and edit standard and device-specific I/O attributes.



	Port Name	Macro Cell	Pin	Fixed	I/O Standard	Output Drive	Slew	Resistor Pull	Input Delay
1	RAM_RAddress[10]	ADLIB:INBUF	3	☐	LVTTL	--	--	None	☑
2	FIFO_AFULL	ADLIB:OUTBUF	2	☐	LVTTL	4	Lo	None	--
3	RAM_RAddress[9]	ADLIB:INBUF	4	☐	LVTTL	--	--	None	☑
4	RAM_WClock	ADLIB:INBUF	1	☐	LVTTL	--	--	None	☑
5	RAM_WAddress[5]	ADLIB:INBUF	3	☐	LVTTL	--	--	None	☑

Figure 2-3. PinEdit's I/O Attribute Editor

Standard Attributes (All Families)

The I/O Attribute Editor shows four standard attributes for all I/O macros:

1. **Port Name** indicates the I/O macro name.
2. **Macro Cell** indicates the type of I/O macro.

3. **Pin #** indicates the current pin assignment.
4. **Fixed**, if checked, indicates that you cannot change the current pin assignment during layout.

Axcelerator Attributes

The I/O Attribute Editor also displays Axcelerator specific attributes. The list below includes a description of Axcelerator specific attributes.

1. **I/O Standard** indicates the I/O standard. Possible I/O standards include LVTTL, LVCMOS 2.5V, LVCMOS 1.8V, LVCMOS 1.5V, 3.3V PCI, LVDS, LVPECL, GTL+, HSTL Class I, SSTL3 Class I and II, and SSTL2 Class I and II. Information on these standards can be found in "Product Support" on page 67. Refer to the appropriate data sheet for information about I/O standards for different families.
2. **Slew** indicates the slew rate for output buffers. Generally, available slew rates are high and low. The output buffer has a programmable slew rate for both high to low and low to high transitions. The slow slew rate is incompatible with 3.3V PCI requirements. For the Axcelerator family, slew can only be edited for the LVTTL I/O standard.
3. **Resistor Pull** indicates the resistor pull: NONE, weak pull-up, Weak pull-down. The default value is NONE. The only exception to this is an I/O that exists in the netlist as a port, is not connected to the core, and is configured as an Output Buffer. In that case, the default setting will be for a weak pull-down.
4. **Hot Swappable** indicates if the pin is hot swappable. The device, the I/O standard specified, and the selected voltage determine this read-only attribute. All the I/O standards except 3.3V PCI are hot-swap compatible and 3.3V tolerant.
5. **Output Load** indicates the output-capacitance value based on the I/O standard selected in the I/O Standard cell.
6. **Input Delay** is set to "on" by checking the box.
7. **Output Drive Strength** can be set to 8, 12, 16, 24 in mA, weakest to strongest. The LVTTL output buffer has four programmable settings of its drive strength. Other I/O standards have full strength.
8. **Bank Name** displays the bank name. This cannot be edited.

SX-A and RTSX-S Family Specific Attributes

The I/O Attribute Editor displays device-specific attributes. Device-specific attributes vary by device and only supported attributes are displayed. The list below includes a description of SX-A and RTSX-S specific attributes.

1. **I/O Standard** indicates the I/O standard. Possible I/O standards include LVTTL/TTL, PCI, CMOS, Custom. Information on these standards can be found in "Product Support" on page 67. Refer to the appropriate data sheet for information about I/O standards for different families.
2. **IO Threshold** indicates compatible threshold level for inputs and outputs, either CMOS, TTL, or PCI.
3. **Slew** indicates the slew rate for output buffers. Generally, available slew rates are high and low. The output buffer has a programmable slew rate for both high to low and low to high transitions. The slow slew rate is incompatible with 3.3V PCI requirements.
4. **Resistor Pull** indicates the resistor pull at power-up time: NONE, weak pull-up, Weak pull-down. This state is of short duration and does not stay. The default value is NONE. The only exception to this is an I/O that exists in the netlist as a port, is not connected to the core, and is configured as an Output Buffer. In that case, the default setting will be for a weak pull-down.
5. **Hot Swap** indicates if the pin is hot swappable. The device, the I/O standard specified, and the selected voltage determine this read-only attribute. All the I/O standards except 3.3V PCI are hot swap compatible and 5V tolerant.
6. **Loading (pf)** indicates the output-capacitance value based on the I/O standard selected in the I/O Standard cell. If you have selected *custom* in the I/O Standard field, you can modify the capacitance value to any integer value that accurately reflects the capacitive loading on the Actel device pins.

ProASIC and ProASIC PLUS Family Specific Attributes

The I/O Attribute Editor also displays device-specific attributes. Device-specific attributes vary by device and only supported attributes are displayed. The list below includes a description of ProASIC ProASIC PLUS and specific attributes.

1. **Loading (pf)** indicates the output-capacitance value based on the I/O standard in the I/O Standard cell. The loading selected is applied to all outputs.

Using the I/O Attribute Editor to Assign I/O Macros

The Pin cell in the I/O Attribute Editor displays the I/O macro's assigned Pin number or "Unassigned" status. If you know the pin number assignment, type the location into this cell. (For information on assigning I/O macros without using the I/O Attribute Editor, see "Use PinEdit to make and edit I/O macro pin assignments. Edits made in PinEdit are permanent, as long as they are fixed and committed (see "Fixing and Committing Pin Assignments" on page 42)." on page 27.)

To assign an I/O macro using the I/O Attribute Editor:

1. **Select the Pin cell for the desired macro in I/O Attribute Editor.**
2. **Enter the pin assignment.** In the Pin cell, type the pin number or select a valid pin assignment from the drop-down list box. The pin assignment is made.

   Note: If you assign a macro to a pin that has already been assigned a macro, the previously assigned macro becomes unassigned. Since PinEdit fixes all assigned macros, the reassignment unfixes the previous assignment.

Using the I/O Attribute Editor to Fix or Unfix Pin Locations

Layout automatically fixes all pins assigned manually and does not alter them. Pins placed by software are unfixed and *should be manually fixed at some point in the design cycle*. Use the I/O Attribute Editor to quickly unfix or fix pins.

A check in the Fixed check box indicates that the selected pin assignment is secure; it will not move during layout (for information on fixing pin locations

without using the I/O Attribute Editor, see "Printing Pin Assignments" on page 30).

To fix a pin location using the I/O Attribute Editor, select the check box in the Fixed column. A check in the check box fixes the pin location. If you want to unfix the I/O macro, unselect the check box.

Specifying an I/O Standard (Axcelerator only)

The I/O Standard column allows you to specify an I/O specification on a per-pin basis.

If required to match the I/O standard, other I/O attributes (such as I/O threshold, slew, loading) will automatically be set to uneditable default settings.

The I/O standards for a generic I/O buffer (only) can be changed to any of the legal I/O standards.

For devices that support I/O banks, the list is restricted to legal choices only. When an I/O is placed, its choice of I/O standards is limited to what the I/O bank location can support. Changing an I/O standard may also unplace existing I/Os. Also, when a macro is assigned an I/O standard, the I/O bank is automatically assigned the voltages VCCI and VREF, if necessary. Unassigning this macro will undo these assignments.

To specify an I/O standard:

1. **Click the *I/O Standard* cell in the desired macro row.**
2. **Specify an I/O standard.** Type or select a supported standard, from the drop down list.

Setting Slew

The default slew displayed in the I/O Attribute Editor is based on the I/O Standard.

The Slew cell indicates the slew rate for output buffers. Generally, available slew rates are high and low. For those devices that support additional slew values, Actel recommends that you use the high and low values and let the software map to the appropriate absolute slew value.

To set slew:

1. **Specify custom I/O Standard.** Select *CUSTOM (*SX-A &RTSX-X) from the I/O Standard cell in the macro row you want to edit.
2. **Set Slew.** Enter the slew or select the slew rate from the Slew list box.

Specifying Capacitance (SX-A and RTSX-S Families)

The default output capacitance appears in the Loading (pf) column of the I/O Attribute Editor. This default value is based upon the I/O specification set in the I/O Standard cell. If necessary, you can change the output capacitance default setting to improve timing definition and analysis. Both the capacitive loading on the board and the Vil/Vih trip points of driven devices affect output-propagation delay. The I/O Attribute Editor provides a mechanism for setting the expected capacitance to improve the propagation-delay model. Timer, Timing Driven Layout, Timing Report, and Back Annotation will automatically use the modified delay model for delay calculations.

To specify capacitance:

1. **Specify custom I/O Standard.** Select *CUSTOM* from the I/O Standard cell in the desired macro row.
2. **Set capacitance in the Loading (pf) column.** You can modify the capacitance value to any integer value that accurately reflects the capacitive loading on the Actel device pins. Increasing capacitance will increase propagation delays.

Specifying I/O Threshold (SX-A and RTSX-S)

The default I/O Threshold displayed is based upon the I/O Standard. If you want to set the I/O Threshold independently of the I/O specification, you must select *CUSTOM* in the I/O Standard cell.

To specify I/O Threshold:

1. **Specify custom I/O Standard.** Select *CUSTOM* from the I/O Standard cell in the macro row you want to edit.
2. **Select IO Threshold.** Select *CMOS*, *TTL*, or *PCI* from the IO Threshold cell. CMOS should be faster on high-to-low transitions, and TTL should be faster on low-to-high transitions.

For input pins, the IO Threshold displays the Input trip point for the pad. This tells the fuser to activate a fuse or not. For output pins, the IO Threshold displays the Output Level of the pad. This does not affect the fuser; however, as with all pads, Timer takes this value into account while calculating delays. For BiBufs (Input/Output pins), the IO Threshold shows the Input trip point and the fuser activates a fuse if needed.

Editing Multiple Rows

To edit multiple rows:

1. **Select the rows to edit.** Click on the column heading to select the entire column, or select specific rows while holding down the CTRL key.
2. **Edit.** While holding down the SHIFT key, select and edit one of the fields. The change occurs in all selected rows.

Sorting I/O Attributes

Use the I/O Attribute Editor to sort I/O macros by attributes. Sort by double-clicking on the attribute column headings.

Fixing and Committing Pin Assignments

Fixing Pin Assignments

Designer does not alter Fixed Pins during Layout. Designer recognizes pins as fixed if they are:

- assigned manually using PinEdit
- assigned in a design schematic
- assigned using a pin file (non-Axcelerator ProASIC families)
- assigned using a PDC file (Axcelerator family only)

Fixed pins are permanent, as long as you commit your fixed pins to your design before you exit PinEdit (see "Closing PinEdit and Committing Pin Assignments" on page 43).

To fix pins:

1. **Select the pin(s) to fix.** Select the pin(s) to fix in the Assigned list box, Package window, or I/O Attribute Editor. To select multiple pins, hold the CTRL key and select multiple pins with your mouse. To select all pins, choose *Select All* from the Edit menu.
2. **Fix the pin(s).** In the Edit menu, click *Fix*. Or, using the I/O Attribute Editor, select the *Fixed* check box.

   Note: If you are using the I/O Attribute Editor, you can only fix one pin at a time.

To unfix a pin:

1. **Select the pin(s) to unfix.** Select the pin(s) to unfix in the Assigned list box, Package window, or I/O Attribute Editor. To select multiple pins, hold the CTRL key and select multiple pins with your mouse. To select all pins, choose *Select All* from the Edit menu.
2. **Unfix the pin(s).** In the Edit menu, click *Unfix*. Or, in the I/O Attribute editor, uncheck the *Fixed* check box.

Closing PinEdit and Committing Pin Assignments

Edits made in PinEdit are only temporary. If you wish to keep your pin assignments and I/O attribute changes, you must commit your changes before closing PinEdit.

Commit changes by selecting the *Commit* command from the File menu or by selecting *Close* from the File menu and clicking *Yes* when asked if you would like to commit changes made in PinEdit.

Committing your changes saves them to the "working" design for this Designer session only. To permanently save changes made in PinEdit to your design file, (`.adb`) you must save your design by choosing *Save* from the File menu in Designer.

Physical Design Constraints (PDC) File (Axcelerator family only)

Physical Design Constraint (PDC) files are TCL script files. PDC files can specify the following:

- I/O standards and features
- VCCI and VREF for all or some of the banks
- Pin locations
- Placement locations
- Net criticality

PDC files can be imported and exported from Designer. Refer to the *Designer User's Guide* for more details.

PDC files replace the PIN file for the Axcelerator family. Non-Axcelerator families do not support PDC files.

PinEdit Scripting Commands

The Designer software allows designers to run scripts in Tcl (Tool Command Language) for simple or complex tasks. You can run scripts from the Windows or UNIX command line or store and run a series of commands in a `.tcl` batch file.

For information on PinEdit Tcl extension commands, please refer to "Scripting" on page 57 of the Designer User's Guide.

A

Product Support

Actel backs its products with various support services including Customer Service, a Customer Technical Support Center, a web site, an FTP site, electronic mail, and worldwide sales offices. This appendix contains information about contacting Actel and using these support services.

Actel U.S. Toll-Free Line

Use the Actel toll-free line to contact Actel for sales information, technical support, requests for literature, Customer Service, investor information, and using the Action Facts service.

The Actel toll-free line is (888) 99-ACTEL.

Customer Service

Contact Customer Service for non-technical product support, such as product pricing, product upgrades, update information, order status, and authorization.

From Northeast and North Central U.S.A., call (408) 522-4480.
From Southeast and Southwest U.S.A., call (408) 522-4480.
From South Central U.S.A., call (408) 522-4434.
From Northwest U.S.A., call (408) 522-4434.
From Canada, call (408) 522-4480.
From Europe, call (408) 522-4252 or +44 (0) 1276 401500.
From Japan, call (408) 522-4743.
From the rest of the world, call (408) 522-4743.
Fax, from anywhere in the world (408) 522-8044.

Actel Customer Technical Support Center

Actel staffs its Customer Technical Support Center with highly skilled engineers who can help answer your hardware, software, and design questions. The Customer Technical Support Center spends a great deal of time creating application notes and answers to FAQs. So, before you contact us, please visit our online resources. It is very likely we have already answered your questions.

Guru Automated Technical Support

Guru is a web-based automated technical support system accessible through the Actel home page (http://www.actel.com/guru/). Guru provides answers to technical questions about Actel products. Many answers include diagrams, illustrations, and links to other resources on the Actel web site.

Web Site

Actel has a World Wide Web home page where you can browse a variety of technical and non-technical information. The URL is http://www.actel.com.

Contacting the Customer Technical Support Center

Highly skilled engineers staff the Technical Support Center from 7:00 A.M. to 6:00 P.M., Pacific Time, Monday through Friday. Several ways of contacting the Center follow:

Electronic Mail

You can communicate your technical questions to our e-mail address and receive answers back by e-mail, fax, or phone. Also, if you have design problems, you can e-mail your design files to receive assistance. We constantly monitor the e-mail account throughout the day. When sending your request to us, please be sure to include your full name, company name, and your contact information for efficient processing of your request.

The technical support e-mail address is **tech@actel.com**.

Telephone

Our Technical Support Center answers all calls. The center retrieves information, such as your name, company name, phone number and your question, and then issues a case number. The Center then forwards the information to a queue where the first available application engineer receives the data and returns your call. The phone hours are from 7:00 A.M. to 6:00 P.M., Pacific Time, Monday through Friday. The Technical Support numbers are:

(408) 522-4460
(800) 262-1060

Customers needing assistance outside the US time zones can either contact technical support via email (tech@actel.com) or contact a local sales office. Please see our list of Worldwide Sales Offices.

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Fax: 407.977.6847

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North Carolina

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