Two-Way Mixed-Voltage Interfacing of Actel's SX FPGAs

Introduction

In the past, bipolar circuits with a 5.0V standard power supply voltage dominated digital system designs. CMOS IC manufacturers adopted this power supply voltage, and most system components are still available in the 5.0V version. In order to achieve even higher speeds and densities at a lower cost and with lower power consumption, the CMOS IC manufacturers have developed advanced deep-submicron fabrication, thinner gate oxides, and process geometries as small as 0.25µm, with 0.18µm expected in 1999.

The disadvantages of designing submicron devices using the 5.0V standard power supply voltage are the resulting high-field-effect failures such as hot-carrier injection. To decrease these failures, a lower supply voltage was needed to power up these new devices, leading to the introduction of the new 3.3V standard power supply voltage devices. This necessitated two-way mixed-voltage interfacing to support the existing 5.0V standard power supply system designs.

This application brief describes the two-way mixed-voltage interfacing specifications available in Actel's SX family of FPGAs. SX devices support two-way mixed-voltage interfacing I/Os that can be used as either regular I/Os or as PCI compliant I/Os. With specific I/O designs, the 54SX16P can meet the two-way mixed-voltage interfacing design requirement. Furthermore, the 54SX16P can be configured to meet the PCI compliant specification. Tables 2, 3, and 4 list the DC electrical characteristics of the SX FPGAs.

TTL Interface Levels

Figure 1 shows the standard TTL (5.0V) and the standard low-voltage TTL (3.3V) DC interface levels that currently exist in a mixed-voltage system. Both standards use the same interface voltage levels.

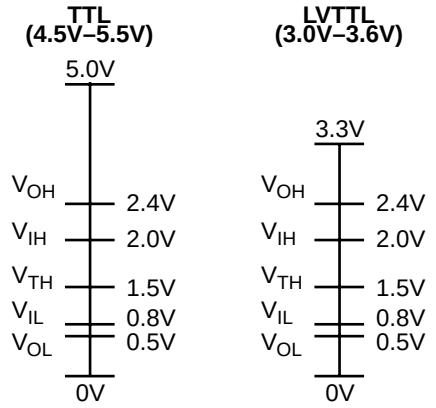

Figure 1 • *5 V (TTL) and 3.3 V (low-voltage TTL) Interfaces*

54SX08, 54SX16, and 54SX32 Operating Mode

To ensure that the 54SX08, 54SX16, and 54SX32 devices can be utilized in different systems, they have been designed to meet various system interface requirements. Table 1 shows the required V_{CCA}, V_{CCI}, and V_{CCR} operating voltages.

The 54SX08, 54SX16, and 54SX32 devices accept LVTTL/TTL signals on all inputs, and the output can drive any LVTTL/TTL devices. The V_{CCA} and V_{CCI} pins must be supplied with 3.3V, while the V_{CCR} pin must be supplied with 5.0V. The outputs are only driven up to 3.3V. Figure 2 shows the operating configuration that is intended for mixed LVTTL/TTL systems.

Table 1 • *SX Operating Configuration*

Description	V_{CCA}	V_{CCI}	V_{CCR}	Vinput Tolerance	Voutput Max
LVTTL/TTL	3.3V	3.3V	5.0V	3.3V/5.0V	3.3V

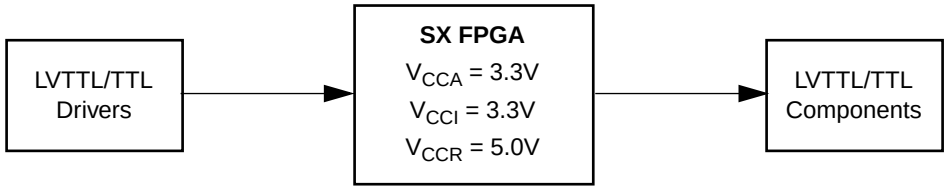

Figure 2 • *SX Operating Mode*

Table 2 • *DC Electrical Characteristics for 54SX08, 54SX16, 54SX32, and 54SX16P*

Symbol	Parameter	Commercial		Industrial		Units
		Min.	Max.	Min.	Max.	
V_{CCA}	Supply Voltage for Array	3.0	3.6	3.0	3.6	Volts
V_{CCI}	IOs Supply Voltage	3.0	3.6	3.0	3.6	Volts
V_{CCR}	Supply Voltage required for internal biasing	4.75	5.25	4.5	5.5	Volts
V_{OH}	I_{OH} = –20 µA (CMOS) I_{OH} = –8 mA (TTL) I_{OH} = –6 mA (TTL)	(V_{CCI} – 0.1) 2.4	V_{CCI} V_{CCI}	(V_{CCI} – 0.1) 2.4	V_{CCI} V_{CCI}	Volts Volts Volts
V_{OL}	I_{OL} = 20 µA (CMOS) I_{OL} = 12 mA (TTL) I_{OL} = 8 mA (TTL)		0.1 0.5		0.5	Volts Volts Volts
V_{IL}	Input Low Voltage		0.8		0.8	Volts
V_{IH}	Input High Voltage	2.0		2.0		Volts

Table 3 • *5V PCI DC Electrical Characteristics for 54SX16P*

Symbol	Parameter and Condition		Commercial		Units
			Min.	Max.	
V_{CCA}	Supply Voltage for Array		3.0	3.6	Volts
V_{CCI}	I/Os Supply Voltage		4.75	5.25	Volts
V_{CCR}	Supply Voltage required for internal biasing		4.75	5.25	Volts
V_{IH}	Input High Voltage		2.0	V_{CCI} + 0.5	Volts
V_{IL}	Input Low Voltage		–0.5	0.8	Volts
I_{IH}	Input High Leakage Current	V_{IN} = 2.7V		70	µA
I_{IL}	Input Low Leakage Current	V_{IN} = 0.5V		–70	µA
V_{OH}	Output High Voltage	I_{OH} = –2 mA	2.4		Volts
V_{OL}	Output Low Voltage I_{OL} = 3 mA (signals without pull up resistor) I_{OL} = 6 mA (signals requiring pull up resistor)			 0.55 0.55	 Volts Volts

Table 4 • *3.3V PCI DC Electrical Characteristics for 54SX16P*

Symbol	Parameter and Condition		Commercial		Units
			Min.	Max.	
V_{CCA}	Supply Voltage for Array		3.0	3.6	Volts
V_{CCI}	I/Os Supply Voltage		3.0	3.6	Volts
V_{CCR}	Supply Voltage required for internal biasing		3.0	3.6	Volts
V_{IH}	Input High Voltage		$0.5V_{CCI}$	V_{CCI} + 0.5	Volts
V_{IL}	Input Low Voltage		–0.5	$0.3V_{CCI}$	Volts
I_{IL}	Input Low Leakage Current	$0 < V_{IN} < V_{CCI}$		±10	µA
V_{OH}	Output High Voltage	I_{OH} = –500µA	$0.9V_{CCI}$		Volts
V_{OL}	Output Low Voltage	I_{OH} = 1500µA		$0.1V_{CCI}$	Volts

54SX16P Operating Modes

The 54SX16P FPGA can be utilized in any system because it has been designed with three operating modes. Table 5 shows the operating modes in which the 54SX16P can be configured to satisfy various system interface requirements.

Mode A (3.3V PCI/LVTTL)

In Mode A, the 54SX16P device accepts 3.3V PCI/LVTTL signals on all inputs, and the output can drive any 3.3V PCI/LVTTL/TTL devices. The V_{CCA}, V_{CCI}, and V_{CCR} pins must be supplied with 3.3V. This mode is intended for 3.3V PCI/LVTTL systems. Figure 3 shows the Mode A configuration.

Mode B (Mixed LVTTL/TTL)

In Mode B, the 54SX16P device accepts LVTTL/TTL signals on all inputs, and the output can drive any LVTTL/TTL devices. The V_{CCA} and V_{CCI} pins must be supplied with 3.3V, while the V_{CCR} pin must be supplied with 5.0V. This mode is intended for mixed LVTTL/TTL systems. Figure 4 shows the Mode B configuration.

Mode C (5.0V PCI/ TTL)

In Mode C, the 54SX16P device accepts 5.0V PCI/LVTTL/TTL signals on all inputs, and the outputs can drive any 5.0V PCI/TTL devices. The V_{CCA} pins must be supplied with 3.3V, while the V_{CCI} and V_{CCR} pins must be supplied with 5.0V. This mode is intended for 5.0V PCI and TTL systems. The output can be driven up to 5.0V. Figure 5 shows the Mode C configuration.

Table 5 • *54SX16P Operating Mode*

Modes	Description	V_{CCA}	V_{CCI}	V_{CCR}	Vinput Tolerance	Voutput Max
A	3.3V PCI/LVTTL	3.3V	3.3V	3.3V	3.3V	3.3V
B	Mixed LVTTL/TTL	3.3V	3.3V	5.0V	5.0V	3.3V
C	5.0V PCI/TTL	3.3V	5.0V	5.0V	5.0V	5.0V

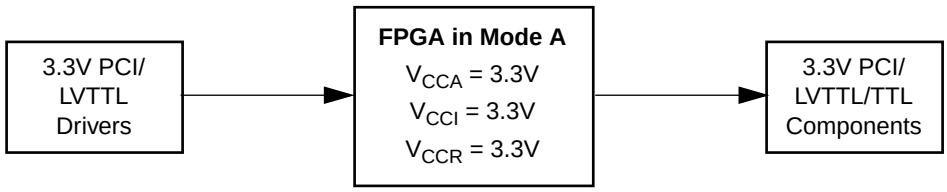

Figure 3 • *Mode A Configuration*

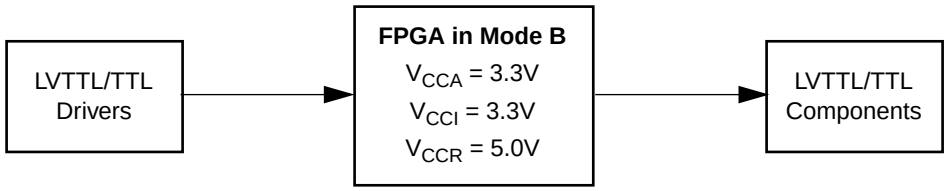

Figure 4 • *Mode B Configuration*

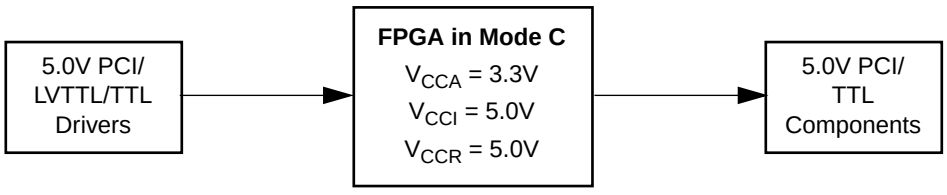

Figure 5 • *Mode C Configuration*

Two-way Mixed-Voltage Interfacing

The 54SX08, 54SX16, and 54SX32 are designed with an N-channel pull-up through the I/Os. The circuit design is shown in Figure 6. The body (well) is grounded, resulting in two virtual diodes. The diodes prevent the forward biasing current, so the I/Os will not be damaged regardless of how the device is powered up or powered down.

The 54SX16P flexible I/Os are designed with a P-channel pull up, as shown in Figure 7. These I/Os can be driven to either 3.3V or 5.0V to support two-way mixed-voltage interfacing. The body (well) is connected to $V_{CCR,}$ which creates two virtual diodes. Therefore, if V_{CCI} is greater than V_{CCR}, damage to the I/Os is possible.

Conclusion

Most systems currently use 5.0V and 3.3V power supply devices. To support this design trend, new devices must support two-way mixed-voltage interfacing. Actel offers a solution with its SX family of FPGAs. The SX FPGAs provide a two-way mixed-voltage interfacing capability that enables the integration of various components operating with different supply voltages.

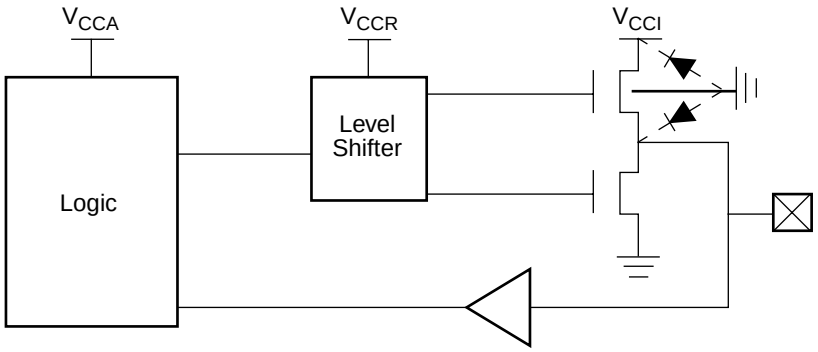

Figure 6 • *SX I/Os with N-channel Pull-up*

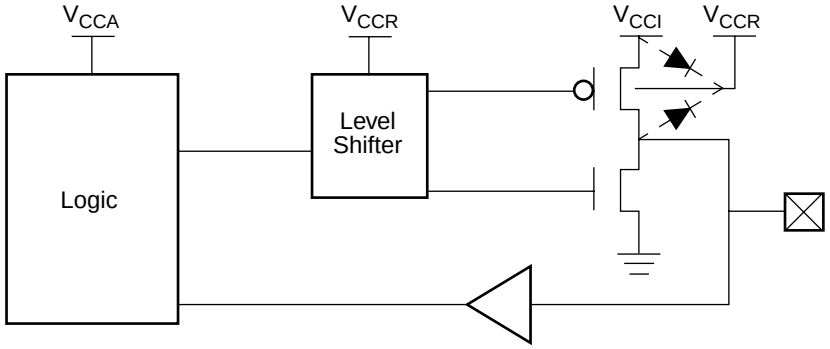

Figure 7 • *SX I/Os with P-channel Pull-up*

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