Power-Up Design Considerations

The state of a system at startup is an important consideration in designing a circuit. It is usually desirable to provide an input signal at startup to reset synchronous circuitry. Otherwise, the system may initially operate in an unpredictable fashion because flip-flops are not designed to power-on in any particular state. Figure 1 shows a typical power-on reset (POR) circuit from which the series resistor, R1, is omitted for TTL circuits.

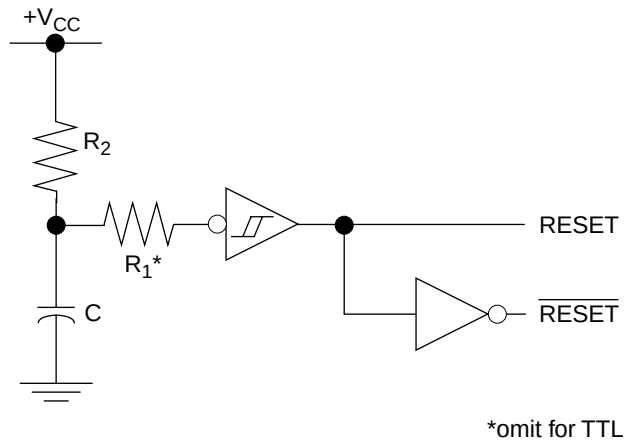

Figure 1 • *Power-On Reset Circuit*

This resistor is necessary with CMOS implementations to prevent damage to the device when power is removed from the circuit. Otherwise, the capacitor would try to power the system via the CMOS input gate protection circuit. A Schmitt trigger (40106, 74LS14) may be advantageous in making the Reset signal switch off cleanly. The hysteresis symbol shown in Figure 1 indicates an inverter with a Schmitt trigger input, such as the CMOS 40106 hex inverter. The following sections describe the power-on conditions of an Actel device and a recommended POR circuit.

Behavior of ACT™ FPGA Inputs

During power-on, the +5 V logic supply rail of a system typically rises from 0 to +5 V in 50 ms or less. Because regulator outputs are usually current limited during this transition, the rise time is more or less linear, with a slope in the range of 0.1 V/ms to 5 V/ms. Each Actel FPGA I/O has a universal pad driver design that may be configured as an input, output, three-state output, or bidirectional input/output. This configuration of the pad driver is accomplished by programming antifuses in the pad driver circuitry.

A single charge pump is used to isolate the 5 V module and the I/O circuits from the interconnect tracks. The interconnect tracks see 15 to 20 volts during programming operations. Such levels would destroy the 5 V modules. The charge pump is essentially a voltage multiplier. As the voltage of Vcc ramps up, the charge pump voltage also ramps up. During ramp-up, the output transistors may source current before the voltage to the input transistors stabilizes. Once stabilized, all I/Os behave as configured.

As the +5 V logic supply rail passes through the region from approximately +1.5 V through +3.0 V, pad drivers that have been programmed as inputs or tristated outputs may behave temporarily as outputs that are in the logical 1 state. Thus, these input pins will temporarily source current into whatever driver is connected to them. They will be sourcing this current from the +5 V logic rail, which at this time is at +1.5 to +3.0 V. This duration is a function of the power rail rise time. For +5 V rails that come up quickly, at 5 V/ms, the duration of the behavior will be approximately 60 µs. For supply rails that rise slowly, at 0.1 V/ms, the duration of the current sourcing behavior will be 3 ms. In the former case, the Actel input can deliver as much as 0.6 µC to the circuit that drives it; in the latter case, the charge is as much as 30 µC. For many driver circuits, this amount of charge is insignificant; however, for others it may be unacceptable.

Inserting a series resistance of sufficient size into the Actel input line can limit the effect of this behavior. In the case of the POR circuit in Figure 2, the series resistance must be chosen to keep $\Delta V \leq 1V$. This guarantees that the POR remains at a logic 0 following the irregularity when the logic supply rail is at approximately 2.5 V, where $\Delta V/\Delta t = i/C$ is the voltage rise time of the capacitor. The capacitor is charged through a resistor to the 5 V logic supply rail, and the diode across the resistor is used to discharge the capacitor at power-off. For a power rail rise time of 0.1 V/ms, the duration of this behavior will be approximately 3 ms. This means that for a POR capacitance of 0.1 µF, the current out of the Actel device input must be limited to

$$i = C\Delta v / \Delta t = (0.1\ \mu F * 1\ V) / 3\ ms = 33\ \mu A$$

which can be achieved using a resistance of 2.24 V/33 mA = 68 kΩ.

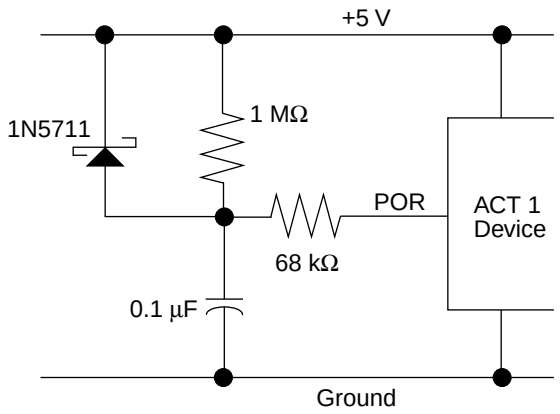

Figure 2 • *Power-On Reset (POR) Circuit with Current-Limiting Resistor*

Furthermore, for drivers that cannot accept a source of current at their outputs or for a multiple-source data bus, it is strongly recommended that the bus drivers be tri-stated during POR.

Characterized Device Behavior During Power-On

Actel devices have been characterized with two V_{CC} rise time conditions—fast power-up and slow power-up. Unless specifically noted otherwise, fast power-up is approximately 0.5 V/µs and slow power-up is approximately 0.2 V/ms. As most power supplies cannot ramp up a PCB board at a rate faster than 0.5 V/µs, Actel has not characterized the behavior of the I/Os at such a rate. During power-up, the I/Os are characterized. Normal input behavior is defined as the input being high impedance (<10 µA leakage). Normal output behavior means the output will either be tristated or be in a predictable state as defined by the logic of the user's design.

Test Circuit

The behavior of inputs and tristated outputs during power-up was characterized by recording the voltage of the inputs and V_{CC} during ramp-up of the supply voltage. Measurements were made in the lab by using socketed parts wire wrapped to V_{CC} and Ground. Power to the test board was supplied using an HP 6825A Bipolar Power Supply. The voltage peak at the inputs was measured without additional load by using an HP 54542C 500 MHz oscilloscope. The HP 10431A 10-to-1 probes represent a load of 6 to 9 pf.

Since the devices were characterized in an isolated socket, measurements in the lab precluded the effects of any other devices that may exist in a typical design. Devices on printed circuit boards (PCB) may experience greater voltage peaks during power-up due to capacitance from the PCB or due to power supply variations. The following data is meant to provide guidance during board-level design. Since each design situation will result in slightly different power-up behavior, it is recommended that the power-up behavior for each Actel device be characterized on the PCB.

ACT 1 Devices

Inputs and outputs will behave normally within 100 µs after V_{CC} reaches 4.75 V with fast power-up and 3.5 V with slow power-up. With fast power-up, inputs remain in a high impedance state. With slow power-up, prior to reaching 3.5 V, inputs will momentarily behave as outputs driving high or low. This happens in about a 0.3 V window between 1 V and 2.5 V. The length of time this high or low level is exerted depends on the rise time of V_{CC}. At 0.2 V/ms, the input went high for about 1 ms and twice went low for about 150 µs each time. Tristated outputs will behave about the same as inputs. Outputs driving high or low will sometimes go to the opposite state (or tristate). Toggling outputs may not perform as expected until V_{CC} reaches 3.5 V. When V_{CC} is between 1.5 V and 3.5 V, I_{CC} will increase to 10–60 mA and then return to normal. The duration is dependent on the V_{CC} rise time, slow power-up being the worst case.

The inputs and outputs of the 3.3 V devices will behave normally within 200 µs after V_{CC} reaches 3 V for fast power-up and within 100 µs after V_{CC} reaches 2 V for slow power-up.

ACT 2/1200XL/3200DX Devices

Normal operation will occur within 100 µs after c reaches 3.5 V for both fast and slow power-up. With slow power-up, inputs and tristated outputs will behave as outputs driving high for approximately 200 µs during a 0.3 V window where V_{CC} is between 1.5 V and 3.0 V. Inputs and tristated outputs stay at high impedance with fast power-up. I_{CC} will rise to 10–50 mA when V_{CC} is between 2 V and 4.5 V and then return to normal.

The 1200XL and 3200DX devices are expected to reach normal operation within 100 µs after V_{CC} reaches 3 V.

RadHard 1280 Devices

Normal operation for I/Os will occur within 200 µs after V_{CC} reaches 3.5 V for slow power-up, less than 1.2 V/ms. During slow power-up, inputs and tristated outputs will behave as outputs driving high for as much as 200 µs while V_{CC} is between 1.5 and 3.0 V. Figure 3 shows the characteristic behavior of an input during slow power-up. When V_{CC} reaches 2.8 V, the input signal peaks at 2.9 V due to capacitive loading. The input signal continues to drive for approximately 60 µs and then resumes normal operation.

Normal operation for I/Os will occur within 100 µs after V_{CC} reaches 5 V for fast power-up, 0.2 V/µs. Figure 4 shows the characteristic behavior of an input during fast power-up. The input peaks at 4.6 V as V_{CC} approaches 5 V. It continues to drive for approximately 60 µs and then returns to normal.

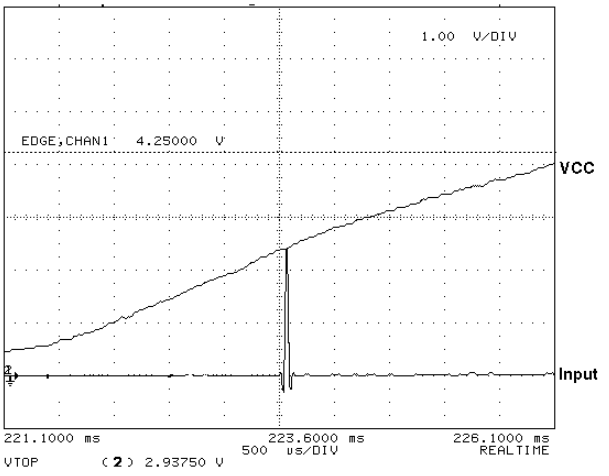

Figure 3 • *Input Behavior under 0 load During Fast Ramp-Up of V_{CC} for the 1280RH Devices*

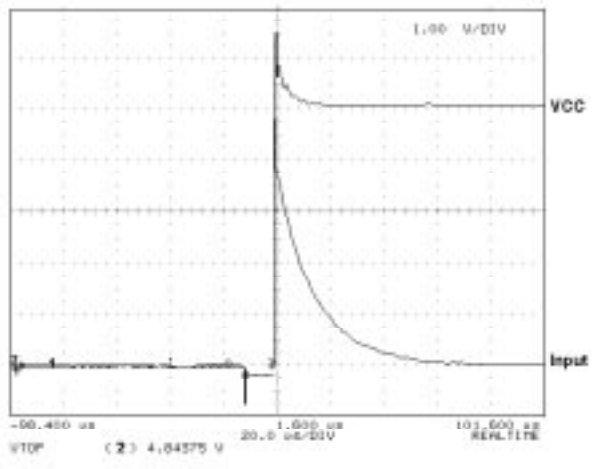

Figure 4 • *Input Behavior under 0 Load During Slow Ramp-Up of V_{CC} for the 1280RH Devices*

ACT 3/ACT 3 PCI Devices

Normal operation for inputs and outputs will occur within 100 µs after V_{CC} reaches 2.75 V. Before reaching the point of normal operation, all inputs and outputs are in a high impedance state (tristate) regardless of V_{CC} rise time. I_{CC} rises to 10–60 mA when V_{CC} is between 2 V and 3 V and then returns to normal.

Summary

Special precautions need to be taken during power-up. Use these methods for avoiding POR problems. The global routed clocks in Actel devices can also be used as resets for synchronous circuits when connected to either Clear or Preset inputs of synchronous macros for the ACT 1 family, and to the Clear inputs for ACT 2, 1200XL, 3200DX, and ACT 3/ACT 3 PCI families.

Actel will continue to characterize the behavior of the ACT family FPGAs. Call Customer Applications at 800-262-1060 for the availability of further device characterizations.

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