Timing Analysis: The Key to High Performance System Logic Design

With the current sets of tools available to designers today, creating a design that is functionally correct is relatively easy. However, achieving required timing is the more challenging task, which requires both skill and experience. Hence, there's a need for fast, accurate, and reliable timing analysis tools to ease the design process and meet timing requirements. Timing tools fall into two categories: dynamic and static. These tools have their own particular strong and weak points in performing timing analysis. Depending on the design's functional complexity both static and dynamic timing analysis might be employed in the design process. Actel tools provide support for the dynamic timing analysis via the Standard Delay File (SDF), and static timing analysis through Actel static timing analyzer (DT Analyze).

These tools address many important design needs. Among these needs is timing estimation, and the other is the need for accurate post-layout data. The goal of this application note is to describe the value of the above mentioned timing needs, and the support that Actel (and other third-party tools) provides to meet these needs.

Timing Estimation

The ability to estimate the performance of a design in its initial stage is invaluable. With the foreknowledge of the design's performance, the designer has an idea of how close the performance of the design is to the target. This helps focus the designer on the element of the design that requires added attention and further modification to meet the timing objectives. At this stage of the design process, the designer can formulate optimization strategies, which employ such techniques as logic duplication and pipelining to achieve the required performance. Logic duplication reduces fan-outs and the use of long routes, especially on critical signals. Also, initial timing information can guide the user on the section of the design that is needed to be constrained when using the timing-driven place and route tool (DirectTime Layout). Thus the appropriate design trade-offs (strategy) can be chosen more effectively with the availability of pre-layout timing data.

Actel's timing analysis tool (DT Analyzer) provides pre-layout timing information to address the need for timing estimation. The user can export from Actel's Designer Series tool pre-layout standard delay files (SDF), which can be used with dynamic simulation. You can also export a pre-layout static timing report, or view the timing data using the DT Analyzer which interactively show the data in tabular form or graphical format as shown in Figure 1**.**

Accurate Post-layout Data

Accurate post-layout data is the key to fewer design iterations. The ability to reflect the hardware characteristic in the tool is necessary to provide and guarantee that the crafted design will perform as expected. Actel's device characteristics have been characterized (data is obtained using the actual hardware as oppose to Spice timing models) to provide the most accurate post layout data for timing analysis.

Dynamic Timing Analysis

Dynamic timing analysis (simulation) has been the standard mechanism in verifying design functionality and performance. Both pre-layout and post-layout timing analysis can be performed via the SDF interface. Pre-layout timing analysis provides quick estimates of the designs performance. Post-layout timing simulation on the other hand provides accurate timing information that is appropriate for device or system level simulation.

Traditional schematic capture tools provide dynamic timing simulators for design verification. Today, there are many vendors that offer dynamic simulators that support language based design entry such as VHDL or Verilog. For example, Cadence's Leapfrog Simulator, Mentor Graphic's Quick(V)HDL Simulator, Model Technology's V-system Simulator, and Viewlogic's SpeedWave simulator are among the many language-based dynamic simulators available in the market.

Static Analysis

Static timing analysis is an exhaustive and convenient method of ensuring that the design meets its timing requirements. There are functions that are especially easy to analyze with the static approach. Complex functions such as a multiplier are much easier to analyze using the static approach because static analysis offers one hundred percent coverage with minimal effort compared to dynamic timing analysis. In addition, the static approach is faster for highly synchronous designs compared to dynamic timing analysis.

Although dynamic timing analysis is very different from static timing analysis, the objective of both analysis tools is one hundred percent test (analysis) coverage. To achieve 100% coverage using dynamic timing analysis is more difficult than static analysis. The difficulty lies in developing simulation vectors that cover all possibilities. Also dynamic timing simulation runs much slower compared to static timing analysis. However it is important to note that there are functions that are much easier to analyze with the dynamic approach than static timing analysis (e.g., asynchronous interactions), and dynamic timing simulation should be performed.

Actel's static analysis tool (DirectTime Analyzer) provides automatic timing reports which include timing data such as internal (external) setup, hold time, and pulse-width requirements. The timing report also includes input-to-output, input-to-register, register-to-output, and clock-to-out delay. The same timing data in the timing report can be viewed interactively and displayed in tabular form using the DirectTime Analyzer graphical user interface (GUI) as shown in Figure 1. This figure shows a path from a clock buffer to an output buffer and the corresponding logic that the path traverses. Detailed delay information is shown in the table, below the chart. With this tool, the designer can easily examine the design's performance margin or deficit.

There are several third-party vendors that offer static timing analysis tools. Mentor Graphics has Quickpath; Synopsys Inc. has VHDLAnalyzer, Teradyne Inc. provides Lasar; and Viewlogic Systems support Motive.

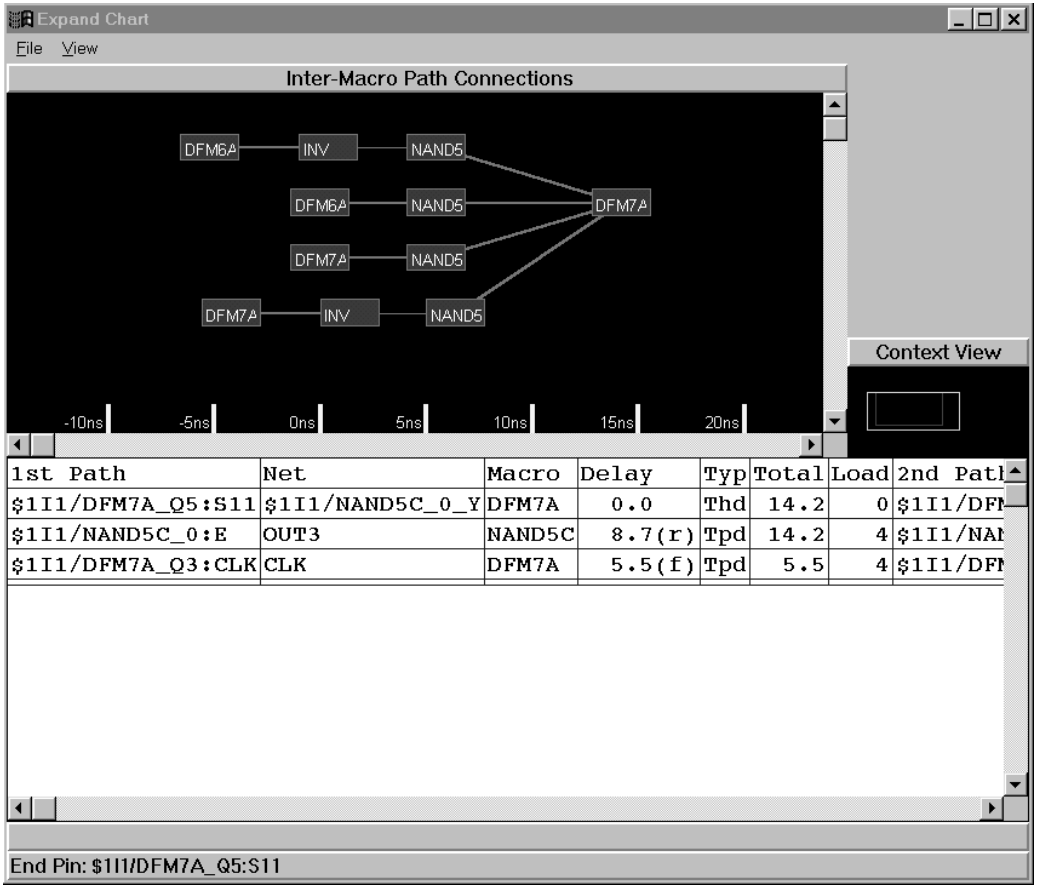

Figure 1 • *Graphical Representation of the Timing Data*

Conclusion

In today's high performance digital designs, achieving timing requirements is a primary key to success. Both static and dynamic timing analysis tools provide solutions in meeting system-timing needs. Actel provides static timing analysis tool and the vehicle to use dynamic timing analysis to perform pre-layout and post-layout simulations. With these tools, designers can perform timing estimation to guide them in making the appropriate design-related decision. And with accurate post-layout timing, designs can be expected to function as intended.

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