Actel® Tools

ChipEdit User's Guide

R1-2003

Windows® & UNIX® Environments

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Trademarks

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Introduction

The ChipEdit tool provides a graphical interface that allows you to view and manually place I/O and logic macros. Like PinEdit, ChipEdit is particularly useful when you need maximum control over your design placement.

Manually placing I/O and logic macros is an optional methodology to help you improve performance and density of a design. It is difficult to outperform Designer's automatic layout process, but if your design requires refining or customizing, ChipEdit provides maximum control to achieve optimum results. ChipEdit is an iterative tool that you can use before and/or after running Layout.

Note: For the Axcelerator family, you must use ChipEdit before running Layout to place I/O FIFO embedded controllers.

Note: ChipEdit does not support the ProASIC and ProASIC ^{PLUS} families. Use the ChipView for ProASIC and ProASIC ^{PLUS} designs. See "Using ChipView" on page 55 for more details.

Use ChipEdit to:

- view macro placements made during layout
- place, unplace, or move macros
- fix I/O macro placements
- view net connections using a ratsnest, minimum spanning tree, or route view
- view architectural boundaries
- view and edit silicon features, such as I/O banks
- cross probe with Silicon Explorer to select probes
- view placement and routing of paths when used with Timer

Document Organization

This guide provides detailed cross-platform information about ChipEdit. Use it as a reference in your everyday work.

Step-by-step instructions for using ChipEdit on Windows and UNIX workstations are in this guide. Any platform differences in procedures and commands are noted in the text.

The ChipEdit User's Guide contains the following chapters:

Chapter 1 - Getting Started with ChipEdit contains details about ChipEdit's interface, toolbars, and menu commands.

Chapter 2 - Using ChipEdit contains instructions on how to use ChipEdit to place macros, view net connectivity, and using ChipEdit with Timer and Silicon Explorer.

Chapter 3 - Using ChipView contains instructions on how to use the ChipView for ProASIC and ProASIC PLUS devices.

Appendix A - Glossary defines key terms used in this manual.

Appendix B - Product Support provides information about contacting Actel for customer and technical support.

Document Assumptions

This document assumes you have a working knowledge of your operating system and its conventions, including standard menus and commands, how to use a mouse, and how to open, save, and close files. For help with any of these techniques, see the documentation that came with your computer.

This document also assumes you are familiar with the FPGA architectures and have a working knowledge of the Designer software.

Your Comments

Actel Corporation strives to produce the highest quality online help and printed documentation. We want to help you learn about our products and get your work done quickly. We welcome your feedback about this guide and our online help. Please send your comments to **docs@actel.com**.

Actel Manuals

Libero includes printed and online manuals. The online manuals are in PDF format and available from Libero's Start Menu and on the CD-ROM.

From the Start menu choose:

- Programs > Libero 2.3 > Libero 2.3 Documentation.
- Programs > Designer Series > R2-2002 Documentation

From the CD, insert your CD-ROM and click *Documentation* from the main screen, or look on the CD-ROM in the "/doc" directory. These manuals are also installed onto your system when you install the Libero software. To view the online manuals, you must install Adobe® Acrobat Reader® from the CD-ROM.

Libero includes the following manuals, which provide additional information on designing Actel FPGAs:

Libero User's Guide. This manual contains information about using Libero, Actel's Integrated Design Environment. Details about using ViewDraw for Actel, WaveFormer Lite, Synplicity, and ModelSim are provided.

Getting Started User's Guide. This manual contains information for using the Designer Series Development System software to create designs for, and program, Actel devices.

Designer User's Guide. This manual provides an introduction to the Designer series software as well as an explanation of its tools and features.

PinEdit User's Guide. This guide provides a detailed description of the PinEdit tool in Designer. It includes cross-platform explanations of all the PinEdit features.

ChipEdit User's Guide. This guide provides a detailed description of the ChipEdit tool in Designer. It includes a detailed explanation of the ChipEdit functionality.

Timer User's Guide. This guide provides a detailed description of the Timer tool in Designer. It includes a detailed explanation of the Timer functionality.

SmartPower User's Guide. This guide provides a detailed description of using the SmartPower tool to perform power analysis.

Netlist Viewer User's Guide. This guide provides a detailed description of the Netlist Viewer. Information on using the Netlist Viewer with Timer and ChipEdit to debug your netlist is provided.

A Guide to ACTgen Macros. This Guide provides descriptions of macros that can be generated using the Actel ACTgen Macro Builder software.

Actel HDL Coding Style Guide. This guide provides preferred coding styles for the Actel architecture and information about optimizing your HDL code for Actel devices.

Silicon Expert User's Guide. This guide contains information to assist designers in the use of Actel's Silicon Expert tool.

Cadence® Interface Guide. This guide contains information to assist designers in the design of Actel devices using Cadence CAE software and the Designer Series software.

Mentor Graphics® Interface Guide. This guide contains information to assist designers in the design of Actel devices using Mentor Graphics CAE software and the Designer Series software.

Synopsys®Synthesis Methodology Guide. This guide contains preferred HDL coding styles and information to assist designers in the design of Actel devices using Synopsys CAE software and the Designer Series software.

Synplicity Synthesis Methodology Guide. This guide contains information about using the Synplicity Synthesis tools with Actel Designer Series software to create designs for Actel devices.

Innoveda® eProduct Designer Interface Guide (Windows). This guide contains information to assist designers in the design of Actel devices using eProduct Designer CAE software and the Designer Series software.

VHDL Vital Simulation Guide. This guide contains information to assist designers in simulating Actel designs using a Vital compliant VHDL simulator.

Verilog Simulation Guide. This guide contains information to assist designers in simulating Actel designs using a Verilog simulator.

Activator and APS Programming System Installation and User's Guide. This guide contains information about how to program and debug Actel devices, including information about using the Silicon Explorer diagnostic tool for system verification.

Silicon Sculptor User's Guide. This guide contains information about how to program Actel devices using the Silicon Sculptor software and device programmer.

Flash Pro User's Guide. This guide contains information about how to program Actel ProASIC and ProASIC PLUS devices using the Flash Pro software and device programmer.

Silicon Explorer II. This guide contains information about connecting the Silicon Explorer diagnostic tool and using it to perform system verification.

Macro Library Guide. This guide provides descriptions of Actel library elements for Actel device families. Symbols, truth tables, and module count are included for all macros.

ProASIC PLUS Macro Library Guide. This guide provides descriptions of Actel library elements for Actel ProASIC and ProASIC PLUS device families. Symbols, truth tables, and tile usage are included for all macros.

WaveFormer Lite Guide. This guide contains information on using WaveFormer Lite to generate VHDL and Verilog stimulus based test benches for the Actel design software.

ViewDraw User's Guide. This guide contains information about using ViewDraw.

ModelSim Bookshelf. This bookshelf contains the ModelSim User's Guide, Command Reference, and Tutorial.

Online Help

Libero comes with online help. Online help specific to each Actel software tool is available for Designer, ACTgen, Silicon Expert, Silicon Explorer II, Silicon Sculptor, and APSW.

1

Getting Started with ChipEdit

This chapter contains details about ChipEdit's interface and commands. For information on using ChipEdit to view, place, and fix macros refer to "Using ChipEdit" on page 29.

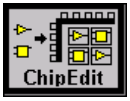
Starting ChipEdit

ChipEdit requires a compiled design. Therefore, you can only invoke ChipEdit for a design (an *.adb file) in a compiled state. If you invoke ChipEdit before compiling your design, Designer will guide you through the compile process before opening ChipEdit.

You must start ChipEdit from Designer. There are three ways to invoke ChipEdit from Designer:

- Choose ChipEdit from the Tools menu, or
- Click the ChipEdit icon in Designer's toolbar, or

- Click the ChipEdit button in Designer's design flow.



ChipEdit starts in a separate window, displaying the logic and I/O modules on the device, as illustrated in Figure 1-1 on page 14.

ChipEdit

ChipEdit, as illustrated in Figure 1-1, consists of multiple specialized windows and tools.

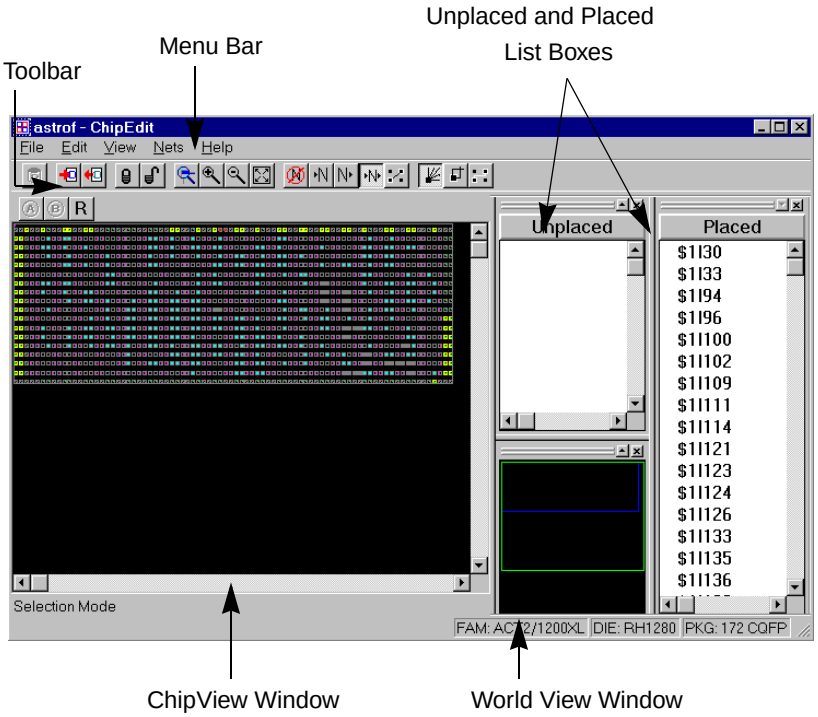


Figure 1-1. ChipEdit

ChipEdit includes a ChipView window, World View window, and Placed and Unplaced list box windows. These windows are highly integrated; anything selected in one is selected or highlighted in all. Commands are accessible from the command menu bar and frequently used commands are on the toolbar.

All the windows and bars are independently sizeable, dockable, and closable. In UNIX, floating windows are not sizeable. To redock or refloat a window, simply double-click the window's title bar.

ChipEdit displays error messages, command functions, and pin information in the status bar.

ChipView Window

ChipEdit's ChipView window displays logic modules and placed macros. When you select a macro in the ChipView window, the macro location is highlighted in the World View window and the macro name is selected in the Placed list box.

To zoom in and out, use the commands in the View menu or toolbar. To use hot keys, place your mouse over the desired zoom area and use Shift and the "+" plus key to zoom in on the location and Shift and the "-" minus key to zoom out.

Colors and Symbols Used in ChipEdit

Colors and symbols are used to differentiate the I/O and logic macros in the ChipView Window. Table A-1 describes the colors and symbols used.

Table A-1. Chip Window Colors and Symbols

Color/Symbol[a]	Definition
White Border	A white border denotes a selected object.
Black Background	A black background denotes an unused or unplaced module.
Blue	Blue denotes a combinatorial module.
Yellow	Yellow denotes *fixed* logic modules. If the module is selected, the symbol appears yellow. If the module is unselected, the border appears yellow.
Green	Green denotes I/O modules.
Red	Red denotes clock modules.
Magenta	Magenta denotes sequential modules.
	Reserved modules that are not user definable are gray, crossed-out symbols on a black background.
	Clock modules are red. Unused/unplaced modules are red symbols on a black background. Used/placed modules are black symbols on a red background.

Table A-1. Chip Window Colors and Symbols (Continued)

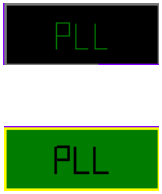
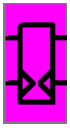
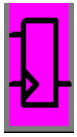
Color/Symbol[a]	Definition
	Input/Output modules are green. Unused/unplaced modules are green symbols on a black background. Used/placed modules are black symbols on a green background.
	Combinatorial modules are blue. Unused/unplaced modules are blue symbols on a black background. Used/placed modules are black symbols on a blue background.
	Sequential modules are magenta. Unused/unplaced modules are magenta symbols on a black background. Used/placed modules are black symbols on a magenta background.
	Buffer modules are blue.
	RAM modules are green. Unused/unplaced modules are green symbols (RAM) on a black background. Used/placed modules are black on a green background.
	PLL modules are green. Unused/unplaced modules are green symbols (PLL) on a black background. Used/placed modules are back on a green background.
	I/O FIFO Block Controller modules are green. Unused/unplaced modules are green symbols (IOFCTL) on black backgrounds. A used/placed module is black on a green background.

Table A-1. Chip Window Colors and Symbols (Continued)

Color/Symbol[a]	Definition
	I/O FIFO Inbuff modules are pink on a black back ground. Used/placed modules are black on a pink background.
	I/O Inbuff modules are pink on a black background. Used/placed modules are black on a pink background.

a. Macros that use more than one module appear as one with a gray background and black symbols.

Color Manager

You can customize the colors used to display I/O banks, clusters, SuperClusters, and nets in the ChipView window.

To customize colors in the ChipView window:

1. **Click *Color Manager* from the View menu.** The color manager dialog box is displayed,as shown in Figure 1-2.

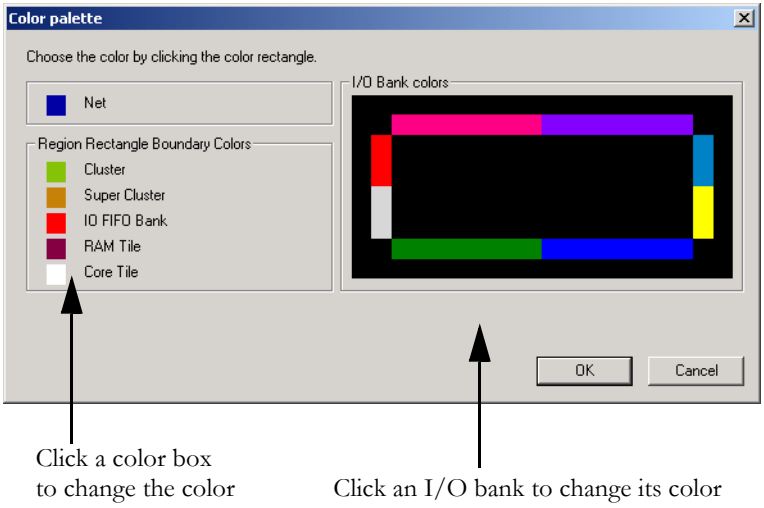


Figure 1-2. Color Manager

2. **Click the color box in front of the item you wish to customize, or click the I/O bank you wish to change.** The color pallet is displayed, as shown in Figure 1-3.

Figure 1-3. Color Choices

3. **Select a color and click *OK*.** The new color appears in the Color Manager dialog box.
4. **After you are done customizing your colors using the Color Manager dialog box, click *OK*.**

World View Window

The World View window's default location is below the Unplaced list box.

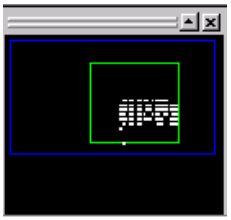


Figure 1-4. World View Window

Use the World View window (Figure 1-4) to control which portion of the ChipView is displayed in the ChipView window. The blue rectangle (known as the ChipView rectangle) represents the chip. The green rectangle (known as the Viewing rectangle) represents the area displayed in the ChipView window.

To move the displayed area to another part of the chip, click the left mouse button and drag the Viewing rectangle to the area on the ChipView rectangle you would like to display. To specify a new display area, click the right mouse button and drag-out a new Viewing rectangle on the ChipView rectangle.

Placed and Unplaced List Boxes

The Placed and Unplaced list boxes display placed or unplaced macros in the design. All placed macros appear in the Placed list box and all unplaced macros appear in the Unplaced list box. Use the Configure List Boxes dialog box (Figure 1-5) to change the default behavior of these list boxes.

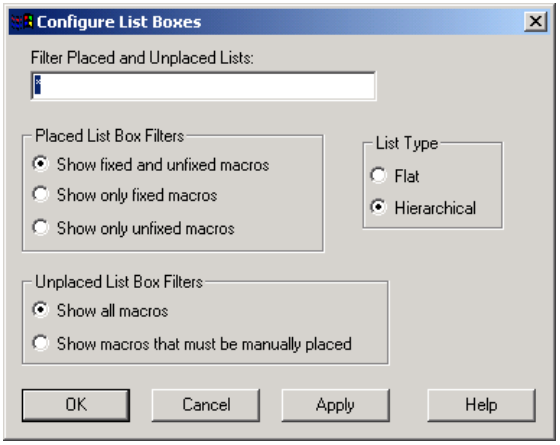


Figure 1-5. Configure List Boxes Dialog Box

ChipEdit displays the Configure List Box dialog box when you choose Configure List Boxes from the View menu.

- **Filter Placed and Unplaced Lists:** Entering a macro name in this area will filter for a specific macro or group to be displayed in the Placed or Unplaced list box. You can use the "*" character as a wildcard.
- **Placed List Box Filters:** Use these radio buttons to filter the Placed List

Box to display fixed and unfixed macros, only fixed macros, or only unfixed macros.

- **UnPlaced List Box Filters**: Use these radio buttons to display all macros or just those that must be manually placed.
- **List Type:** Use the List Type filters to display macro instance names in a flat or hierarchical list in the Placed and Unplaced list boxes. When instance names are displayed hierarchically, collapsed levels are preceded by a plus sign (+) and expanded levels are preceded by a minus sign (-). Clicking the plus sign expands the hierarchy of a macro, while clicking the minus sign collapses the hierarchy. Macros, both fixed and unfixed, are displayed hierarchically by default.

ChipEdit Toolbar

The ChipEdit toolbar contains commands for performing common ChipEdit operations on your designs. Click a button in the toolbar to execute a command.

Table A-1. ChipEdit Toolbar

Toolbar Button	Function
	Save
	Place
	Unplace

Table A-1. ChipEdit Toolbar

Toolbar Button	Function
	Fix
	Unfix
	Zoom Area
	Zoom in
	Zoom Out
	Fit in the Window
	Configure List Boxes
	No Nets

Table A-1. ChipEdit Toolbar

Toolbar Button	Function
	Nets in
	Nets out
	Nets in and out
	Selection only
	Ratsnest
	Minimum Spanning Tree
	Routing

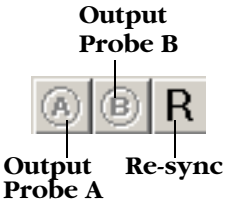


Figure 1-6. Silicon Explorer Toolbar

If you position the mouse pointer over a toolbar button, a short description called a tool-tip appears. A longer description appears in the status bar at the bottom of the main window.

ChipEdit's toolbar is floating. This means you can drag it to any edge of the window, or by dragging it from any edge, you can leave it floating over your work. To avoid clicking toolbar buttons by mistake, drag the toolbar from its separator bar.

ChipEdit Menu Commands

The PC and UNIX versions of ChipEdit have the same menus. However, some dialog boxes may look slightly different on the two platforms due to the different window environments. The functionality is the same on both platforms, though the locations of the fields and buttons on the dialog boxes may vary. The names of some fields may also vary between the PC and UNIX versions.

File Menu

Commit: Saves the macro placements into the database.

Print: Prints macro placements.

Close: Closes the ChipEdit window.

Edit Menu

Place: Places selected macro in the next selected module location.

Unplace: Unplaces the selected macros.

Fix: Fixes the selected macro in the designated location.

Unfix: Unfixes the selected macro.

Select All: Selects all macros.

Select All Placed: Selects all placed macros.

Select All Unplaced: Selects all unplaced macros.

Configure I/O Banks: Opens the Configure I/O Banks dialog box.

View Menu

Zoom Area: Enlarges a user-defined rectangular region of the design.

Zoom In: Enlarges by a scale of 2x.

Zoom Out: Decreases by a scale of .5x.

Fit in Window: Fits the entire design view in the ChipView window.

Redraw: Refreshes the ChipView window.

Mark Location: Marks your cursor location, which you can return to by selecting *Return to Mark*.

Return to Mark: Returns you to your last marked location.

Configure List Boxes: Filters what is displayed in the list boxes.

Color Manager: Opens the Color Manager dialog box.

Static Objects: Options in the sub-menu depend upon the family. (Only for SX, SX-A, eX, and Axcelerator.)

View I/O Banks: Hides or displays the I/O Banks.

Toolbar: Hides or displays the toolbar.

Placed List Box: Hides or displays the Placed List Box.

Unplaced List Box: Hides or displays the Unplaced List Box.

World View: Hides or displays the World View Window.

Status Bar: Hides or displays the status bar.

Nets Menu

Display: Use options in the sub-menu with the ratsnest or minimum spanning-tree modes.

- **None**: Hides nets.
- **Input**: Displays input nets.
- **Output**: Displays output nets.
- **Both**: Displays input and output nets.
- **Selection Only**: Limits the ratsnest to show nets between selected modules only.

Display Algorithm: Use with the following net display options: input, output, or both.

- **Ratsnest**: Activates ratsnest view mode.
- **Minimum Spanning Tree**: Activates minimum spanning-tree view mode.
- **Routes:** Displays routing.

Select Net: Locates a net by name.

Show Net Details: Displays detailed information about a net.

Help Menu

Help Topics: Starts Online Help.

Reference Manual: Displays ChipEdit User's Manual (PDF).

Extended Error Messages: Displays a dialog box with detailed information on the error message.

Status Bar

Family, die and package information appears in the right corner of the status bar. In addition, the status bar displays information on commands, pins, placed macros, nets, error messages, and the family, die, and package.

- Hold your mouse over a placed macro in the ChipView window to see the pin number, instance name, net name, macro cell, and fixed or unfixed status in the Status Bar.

- To see nets displayed in the status line, select a macro, zoom in, and click one of the ratsnest lines.
- If you hold your mouse over a toolbar icon or a menu command, a short description of the command function appears in the Status Bar.

Error messages (Figure 1-7) in the Status Bar provide details about invalid placement attempts. Choose Extended Error Messages from the Help menu to view more information about the last failed command or placement attempt.

Figure 1-7. Extended Error Messages

2

Using ChipEdit

The ChipEdit tool provides a graphical interface that allows you to customize your macro placement. Use ChipEdit to place macros, to view macro placements, and to view the connectivity between macros. ChipEdit can also be used along with Timer and Silicon Explorer to optimize and verify your design.

Generally, ChipEdit is an iterative tool that you can use before and/or after running Layout. However, for the Axcelerator family, you must use ChipEdit before running Layout to place I/O FIFO Embedded Controllers.

For a complete description of ChipEdit's interface and menu commands, see "Getting Started with ChipEdit" on page 13.

Making Macro Assignments

Use ChipEdit to place, unplace, and edit the placement of I/O and logic macros in your design. Edits made in ChipEdit are permanent when the macro placements are fixed and committed (see "Fixing Macro Placements" on page 34 and "Committing Macro Placements" on page 35).

Note: For the Axcelerator family, you must use ChipEdit to place I/O FIFO Embedded Controllers before running Layout.

Placing Macros

To place a macro:

1. **Start ChipEdit.** Click the ChipEdit button in Designer's Design Flow window (see "Starting ChipEdit" on page 13).
2. **Select the macro to be placed.** Select the macro to be placed in the Unplaced list box.
3. **Place the macro.** There are three ways to place macros:
   - **Drag and Drop:** Drag the selected macro name from the Unplaced list box to the module location in the ChipView Window. Valid module locations are high-lighted in the ChipView Window.
   - **Menu Commands**: In the Edit menu, click *Place* and then select a module location in the ChipView Window.
   - **Toolbar Commands**: Click the Place icon and then select the module in the ChipView window.

If the macro placement is valid, the macro is placed. Error messages in the status bar notify you about invalid placement attempts. Choose Extended Error Messages from the Help menu for more details on a specific error message. If you want to ensure that the macro is not moved during layout, you must fix the macro placement and commit your changes when exiting ChipEdit.

Note: Placing a macro in a module that already has a macro will unplace the previously placed macro, even if its placement has been fixed.

Placing Multiple Macros

To make multiple macro placements, place the macros as a group.

To place multiple macros:

1. **Select the macros to be placed.** While holding down the CTRL or SHIFT key, select multiple macros in the order you want them placed.
2. **Activate the Place mode.** In the Edit menu, click *Place*.
3. **Select module placements in the ChipView window.** The macros will be placed in the order selected.

Unplacing Macros

Unplace a macro if you find that its placement is no longer necessary. Unplaced macros are automatically placed during layout.

To unplace a macro:

1. **Select the macro in the Placed list box or ChipView window.**
2. **Unplace the macro.** Unplace the selected macro using any one of the following methods:
   - **Keyboard:** Press the delete key.
   - **Drag and Drop**: Drag the selected macro name from the Placed list box to the Unplaced list box.
   - **Menu Commands**: In the Edit menu, click *Unplace*.
   - **Toolbar**: Click the Unplace icon.

The macro is unplaced and the instance name appears in the Unplaced list box.

To unplace multiple macros:

1. **Select macros to unplace.** To select multiple macros in the Placed list box, hold down the CTRL or SHIFT key and select the macros with your mouse. To select all macros, choose Select All from the Edit menu.
2. **Unplace the macros.** In the Edit menu, click *Unplace*. All selected macros are unplaced.

Moving Macros

You can move macros that have been placed manually using ChipEdit or automatically during layout using ChipEdit.

To move a placed macro:

1. **Select the macro to move.** Select the macro name in the Placed list box or select the macro in the ChipView window.
2. **Move the macro. Drag and drop the selected macro to the new logic or I/O module in the ChipView window.**

Placing RAM or FIFO Blocks

RAM and FIFO Blocks are placed in RAM modules on the chip.

To place RAM or FIFO blocks:

1. **Start ChipEdit.** (For more information, refer to the *Designer User's Guide*.)
2. **Activate the SuperCluster view.** From the View menu, choose *Static Objects* and click *SuperCluster Rect*.

3. **Zoom in and locate a RAM module, as shown in Figure 2-1.**

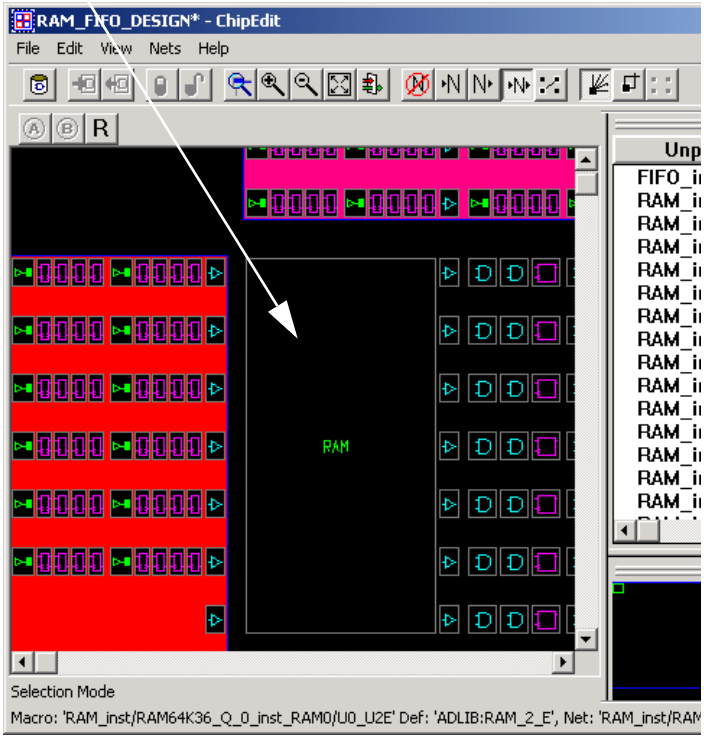


Figure 2-1. Memory Cluster (Axcelerator Family)

4. **Select the RAM or FIFO block in the Unplaced window and drag and drop it onto one of the empty RAM modules.** All the RAM or FIFO macros in the block are placed in the nearest legal locations.

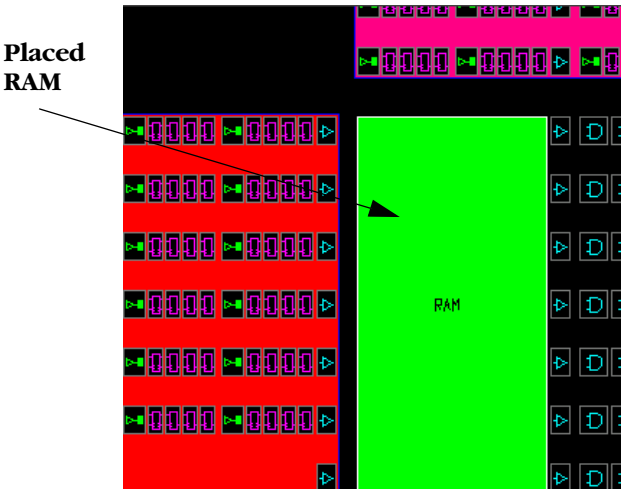


Figure 2-2. Placed RAM in Memory Cluster

5. **After placing all RAM or FIFO blocks, you must fix the placements.** From the Edit menu, click *Fix*. (For more information on fixing macro placements, refer to "Fixing Macro Placements" on page 34.

6. **Commit and Exit ChipEdit.** From the File menu, click *Exit*. When prompted to commit your changes, click *Yes*. Committing saves your placements to Designer's temporary design file.

Placing I/O FIFO Embedded Controllers

Manual placement of I/O FIFO Embedded Controllers before running Layout is required for the Axcelerator family.

Every I/O can have a dedicated FIFO with a fixed depth of 64 bits. Each I/O FIFO can be individually controlled; in which case the flag logic has to be built into the FPGA. Alternatively, you can use an I/O FIFO Embedded Controller to control sets of I/O modules for bus applications.

I/O FIFO Embedded Controller Considerations:

1. All I/Os with a dedicated FIFO that is controlled by the same I/O FIFO Embedded Controller must be placed in the same block as the I/O FIFO Embedded Controller.
2. All I/Os with a dedicated FIFO that is individually controlled can be placed anywhere.
3. You cannot mix I/Os with a dedicated FIFO that is controlled by different I/O FIFO Embedded Controllers in the same I/O FIFO Block.
4. The I/O FIFO Embedded Controllers must be placed before running Layout. They cannot be automatically placed.
5. The above does not change the banking rules (i.e. any I/Os placed in a bank must have compatible technologies).
6. While the I/O FIFO or I/O FIFO Embedded Controller does not have a technology requirement, the I/O that contains the dedicated FIFO does.

To place an I/O FIFO Embedded Controller:

1. **From the View menu, click *Static Objects* and select *I/O FIFO Block* from the sub-menu.** Borders around each I/O FIFO block appear. The colors used for borders can be changed see "Color Manager" on page 17.

   Each I/O bank can have 1 or more I/O FIFO blocks. Each block only has one I/O FIFO embedded controller.

2. **Select the I/O FIFO Embedded Controller in the Unplaced list box.**
3. **Drag and drop it into an I/O FIFO Embedded Controller module in the ChipView Window.**

Fixing Macro Placements

Use ChipEdit to fix macro placements. Fixed macros are not moved during Layout. Fixed macros only become permanent when you commit them before exiting ChipEdit (see "Committing Macro Placements" on page 35).

To fix macros:

1. **Select the macro(s) to fix.** Select the macro(s) to fix in the Placed list box or ChipView window. To select multiple macros, hold the CTRL key and select multiple macros with your mouse. To select all macros, choose Select All from the Edit menu.
2. **Fix the macro(s).** From the Edit menu, click *Unfix*.

To unfix a macro:

1. **Select the macro(s) to unfix.** Select the macro in the Placed list box or ChipView window. To select multiple macros, hold the CTRL key and select multiple macros with your mouse. To select all macros, choose Select All from the Edit menu.
2. **Unfix the macro(s).** In the Edit menu, click *Unfix*.

Committing Macro Placements

Edits made in ChipEdit are only temporary until committed. To save your changes, commit your changes before exiting ChipEdit.

Commit changes by choosing the Commit command from the File menu or by exiting ChipEdit and selecting Yes when asked if you would like to commit changes made in ChipEdit.

Committing your changes saves the changes to the temporary design stored in Designer. If you wish to permanently save the changes made in ChipEdit to your design .adb file, you must save your design in Designer by choosing Save from the File menu.

Printing the ChipView Window

To print the contents of the ChipView window:

1. **In the File menu, click *Print*.** The Printer dialog box is displayed.
2. **Select your printer options and click *OK*.**

For information on setting up a printer in UNIX, please refer to the *Designer User's Guide*.

I/O Banks

For devices that support multiple I/O standards, I/Os are grouped onto I/O banks around the chip. For the Axcelerator Family, there are 8 I/O banks surrounding the chip, two per-side, numbering 0-7. The I/O banks are color coded for quick identification. Colors can be customized using the Color Manager.

Each I/O bank has a common VCCI, the supply voltage for its I/Os. Each I/O bank also has a common reference voltage bus, VREF for the voltage-referenced I/O standards. Only one VREF value can be assigned to each I/O bank. Only I/Os compatible with both the same VCCI and VREF standards can be assigned to the same bank.

Table 2-1 shows compatible I/O standards

Table 2-1. Legal I/O Usage Matrix

I/O Standard	LVTTL 3.3V	LVCMOS 2.5V	LVCMOS1.8V	LVCMOS1.5V (JESD8-11)	3.3V PCI 3.3V, PCI-X	GTL + (3.3V)	GTL + (2.5V)	HSTL Class I	SSTL2 Class I & II	SSTL3 Class I & II	LVDS 2.5V ±5%	LVPECL (3.3V)
LVTTL 3.3V (V_{REF}=1.0V)	X				X	X						X
LVTTL 3.3V (V_{REF}=1.5V)	X				X					X		X
LVCMOS 2.5V (V_{REF}=1.0V)		X					X					
LVCMOS 2.5V (V_{REF}=1.25V)		X							X			
LVCMOS1.8V			X									
LVCMOS1.5V (V_{REF}=1.75V) (JESD8-11)				X				X				
PCI 3.3V, PCI-X (V_{REF}=1.0V)	X				X	X						X
PCI 3.3V, PCI-X (V_{REF}=1.5V)	X				X					X		X
GTL + (3.3V)	X				X	X						X
GTL + (2.5V)		X					X					
HSTL Class I				X				X				
SSTL2 Class I & II		X							X		X	
SSTL3 Class I & II	X				X					X		X
LVDS (V_{REF}=1.0V)		X					X				X	
LVDS (V_{REF}=1.25V)		X							X		X	
LVPECL (V_{REF}=1.0V)	X				X	X						X
LVPECL (V_{REF}=1.5V)	X				X					X		X

If standards can be used within a bank at the same time, you will find a “X” in the table.

Examples:

a) LVTTL can be used together with itself, PCI3.3V, PCI-X, and GTL+ (3.3V), when VREF = 1.0V (GTL+ requirement).
b) LVTTL can be used together with itself, PCI3.3V, PCI-X, and SSTL3 Class I & II, when VREF = 1.5V (SSTL3 requirement).

To assign technologies to I/O banks:

1. **Select an I/O bank.**
2. **From the Edit menu, click *Configure I/O Banks*.** The Configure I/O Banks dialog box is displayed, as shown in Figure 2-3.

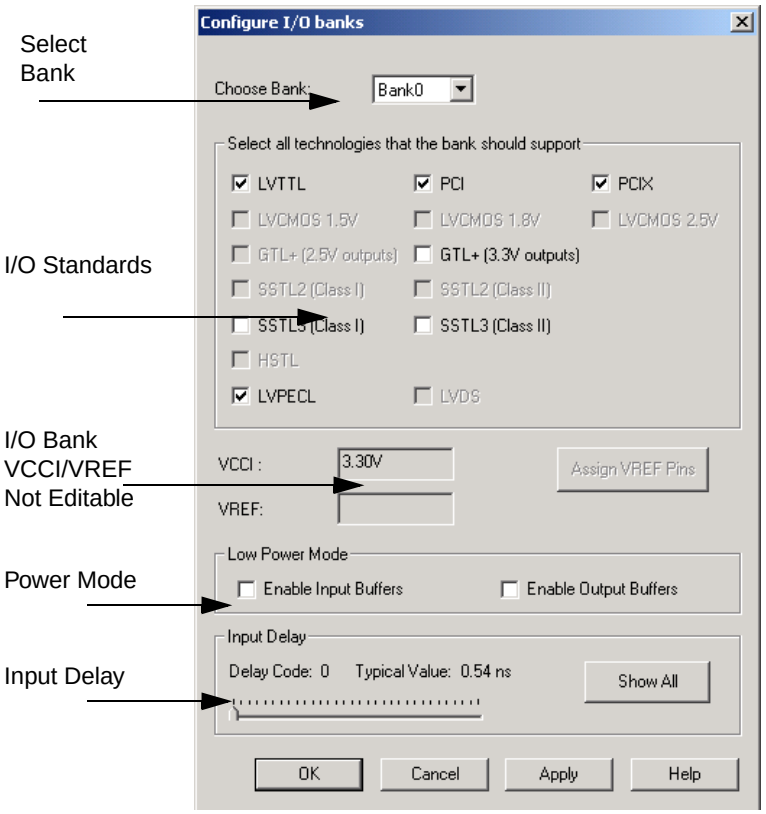


Figure 2-3. Configure I/O Banks Dialog Box

- **Select Technologies**: Selecting a standard selects all compatible standards and grays out incompatible ones. For example, checking LVTTL will check PCI, PCIX, and LVPECL, since they all have the same VCCI. Further selecting GTL (3.3V) disables SSTL3 as an option because the VREFs of the two are not the same.
- **Assign VREF Pins**: After you have selected your technology, click *Apply*. If VREF pins are required, this button becomes activated. Click to assign VREF pins. You must assign VREF pins at least once.
- **Low Power Mode** (Optional): Select Enable Input Buffers or Enable Output Buffers.
- **In Delay**: Drag the slider bar to your desired delay. The delay is bank specific. Drag the meter to your desired delay index. The delay code and typical value appear. Click *Show All* to see all the delay values (Best, Worst, Typical, Rise-Rise, Fall-Fall). A technology must be selected in order to see the input delays. Click *OK* to dismiss the Show All Delays dialog box.

3. **Make your selections and click *Apply*.** The I/O bank is assigned the selected standards. Any I/O of the selected types can now be assigned to that I/O bank. Any previously assigned I/Os in the bank that are no longer compatible with the standards applied are removed.

   If VREF pins can be assigned, the Assign VREF Pins button will highlight.

4. **Assign I/O standards to other banks by selecting banks from the list and assigning technologies.** Any banks not assigned I/O standards use the default standard selected in the Device Selection Wizard.

5. **When you are done, click *OK*.** Proceed to assign I/Os with the same standards to the appropriate banks. (See the *PinEdit User's Guide* for more information.**)**

Assigning VREF Pins

Voltage referenced I/O inputs require an input referenced voltage (VREF).

To assign VREF pins:

1. **From the Edit menu, click *Assign I/O Technologies to I/O Banks*.**
2. **Specify the supported technologies for the I/O bank and click *OK*.**
3. **If VREF pins can be assigned, the Assign VREF Pins button activates.**
4. **Click *Assign VREF Pins*.** The Assign VREF Pins dialog box appears, as shown in Figure 2-4.

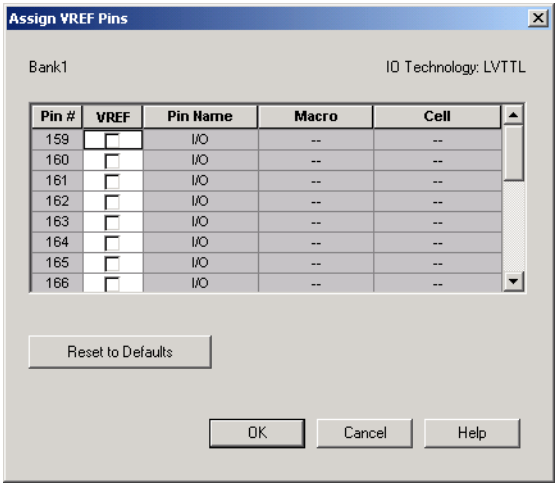


Figure 2-4. Assign VREF Pins Dialog Box

5. **Check the VREF box next to the pin number and click *OK*.** Click the *Reset to Defaults* button to revert to Actel recommended defaults.
6. **Click *OK* in the Assign I/O Technologies to I/O Banks dialog box.**

Specifying I/O Bank Voltages

You can directly specify voltages for each I/O bank by doing one of the following:

- Using the Assign Technologies to I/O Banks dialog box
- Placing an I/O of a particular technology in an I/O bank that has not been assigned a voltage.
- Using the command 'set_iobank' in the Physical Design Constraints (PDC) File.

I/O Bank Voltage Assignments using the Assign Technologies to I/O Banks Dialog

Bank voltages must be set before running Layout (place and route).

You can assign voltages to an I/O Bank using the Assign I/O Technologies dialog box, see "I/O Banks" on page 36. When voltages are assigned, any previous I/O assignments not compatible are removed from the bank, appearing back in the unassigned column.

I/O Bank Voltage Assignments by Assigning I/O Macros

When you assign an I/O macro, the legality is checked according to the I/O Bank rules. It may sometimes happen that a pin occupying a VREF location will come in the way of placing a voltage referenced I/O. In this case, the I/O occupying the VREF will need to be unassigned first.

When a bank is without any voltage assignments, the I/O macros assigned to the bank will decide the voltages. These assignments will be undone if the macros in the bank become unassigned.

It is also possible to assign an I/O technology to an already assigned macro through the I/O attribute editor by changing the I/O standard, see "Specifying an I/O Standard (Axcelerator only)" on page 40 in the *PinEdit User's Guide*. This assigns voltages to the entire bank (a bank can only support one voltage).

Viewing Nets and Connectivity

ChipEdit displays the nets and their connectivity between logic modules in the ChipView window. Net connectivity can be displayed three ways- a ratsnest view, a minimum spanning tree view, or, if route has been completed, then the actual routes.

A ratsnest view is a display of connections between placed logic macros. The minimum spanning tree view shows the minimum paths between connected macros. The route view shows the actual routes used to connect macros.

You can also locate nets by name.

Ratsnest View

The ratsnest view displays net connectivity between placed logic macros by connecting lines from the output pins to all input pins in the ChipView window. Use the ratsnest to understand how logic macros are connected to each other. The ratsnest view is activated by default, showing all input and output nets for selected macros.

To turn on the ratsnest view:

1. **Turn on the types of nets to display.** Choose input, output, or both from the Nets menu or click the corresponding Net toolbar icon.
2. **Activate the ratsnest view.** From the Nets menu, click *Display Algorithm Ratsnest* or click the Ratsnest icon in the toolbar.
3. **Select the placed macro in the ChipView window or Placed list box.** Select multiple macros by holding down the CTRL key while

selecting macros ChipEdit displays the ratsnest in the ChipView window, as seen in Figure 2-5.

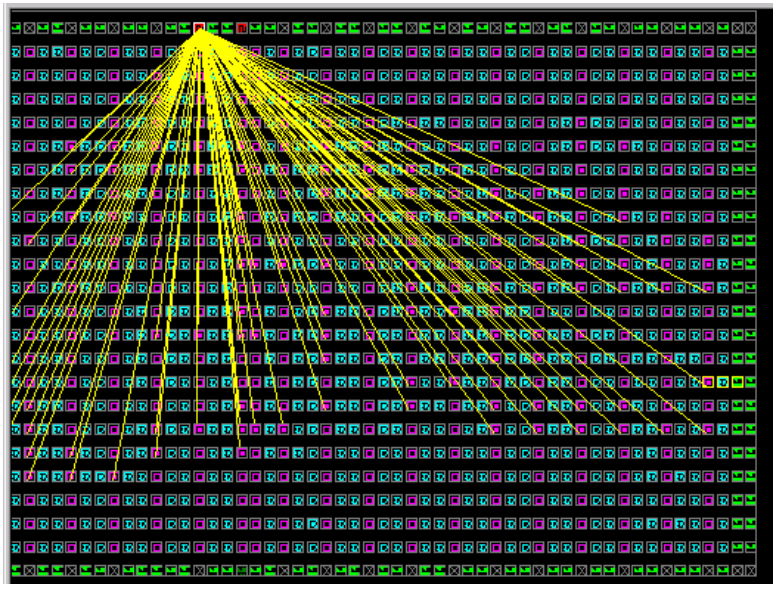


Figure 2-5. Ratsnest Mode

Left on, the ratsnest view continues to display nets between macros as you place I/O and logic macros.

To turn off the net display, click the None Nets button in the toolbar or choose *None* from the Nets Display sub-menu.

Minimum Spanning Tree View

The minimum spanning tree view displays net connectivity using the shortest paths between placed macros.

To display the minimum spanning tree view:

1. **Turn on the types of nets to display.** Choose *input*, *output*, or *both* from the Nets menu or click the corresponding Net toolbar icon.
2. **Activate the minimum spanning tree view.** From the Nets command menu, select *Display Algorithm* and click *Minimum Spanning Tree* or click the minimum spanning tree button in the toolbar.
3. **Select the placed macro in the ChipView window or Placed list box.** Select multiple macros by holding down the CTRL key while selecting macros. ChipEdit displays the minimum spanning tree in the ChipView window, as seen in Figure 2-6.

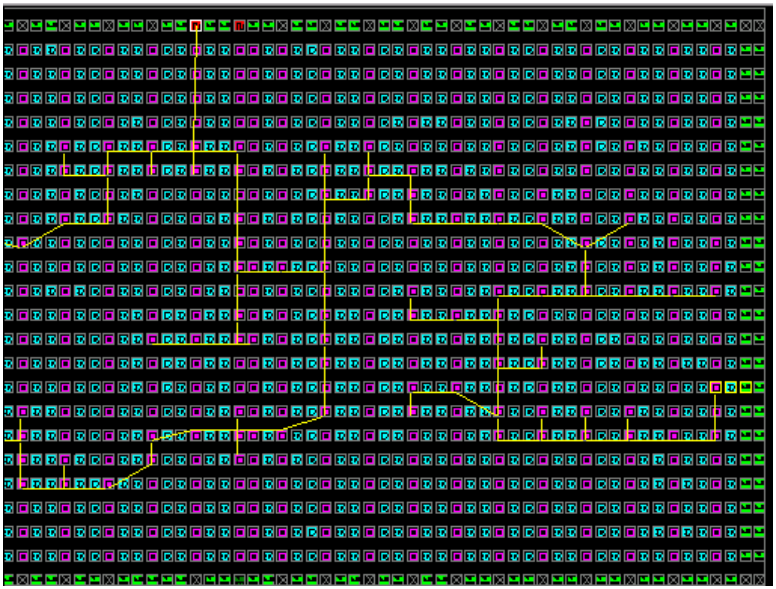


Figure 2-6. Minimum Spanning-Tree Mode

The minimum spanning tree view will continue to display connectivity between selected macros as you place I/O and logic macros.

To turn off the net display, click the None Nets button in the toolbar or choose *None* from the Nets Display sub-menu.

Route View

The route view displays a representation of the actual routes used to connect placed macros. This feature helps show the general location of routing segments used by the design.

To activate the routes view:

1. **Complete Layout before running ChipEdit.** To display routes, Layout must be completed before running ChipEdit.
2. **Turn on the types of nets to display.** Choose *input*, *output*, or *both* from the Nets menu or click the corresponding Net toolbar icon.
3. **Activate the route view.** From the Nets menu, choose Display Algorithm Routes or click the routes icon in the toolbar.
4. **Select the placed macro in the ChipView window or Placed list box.** Select multiple macros by holding down the CTRL key.

Note: If a macro is moved or unplaced, then the nets connected to that macro will be displayed using a ratsnest.

Locating a Net by Name

To locate a net by name:

1. **From the Net menu, click *Select Net.*** The Select Net dialog box is displayed, as shown in Figure 2-7.

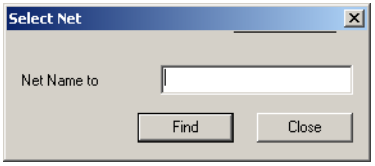


Figure 2-7. Select Net dialog box

2. **Enter Net name and click *Find.*** The net is highlighted in the ChipView window, as shown in Figure 2-8.

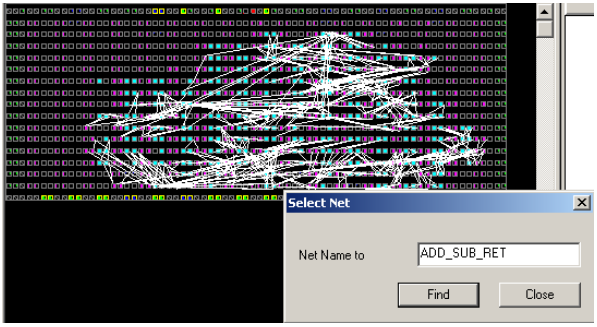


Figure 2-8. Selected Net Highlight in the ChipView window

Displaying Net Details

To display net details:

1. **Select a net or locate the net by name.** See "Locating a Net by Name" on page 46.
2. **From the Net menu, click *Show Net Details*.** The Net Details dialog box, as shown in Figure 2-9,displays pin name and xy coordinates

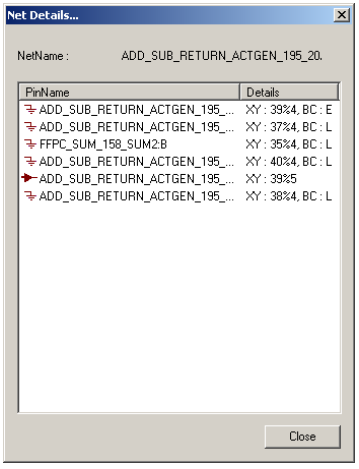


Figure 2-9. Net Details dialog box

Viewing Static Objects

Clusters and SuperClusters

Clusters and SuperClusters can be viewed by using the Static Object viewing mode.

A cluster is a group of logic elements. Which elements make up the group is determined by the type of device. A SuperCluster is at least 2 clusters (SX) or 2 clusters and a buffer (Axcelerator). Modules in a cluster can be connected by fast or direct connects.

You can hide or display this viewing mode.

Note: This feature is only available for the SX, SX-A, eX, and Axcelerator families.

To view clusters or SuperClusters:

1. **From the View menu, select *Static Objects* and click *Cluster Rect.* or *SuperCluster Rect.*** The cluster areas appear in the ChipView window, as seen in Figure 2-10**.**

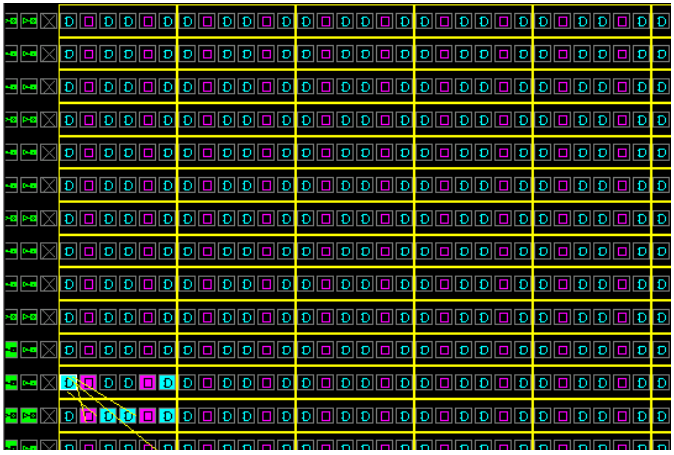


Figure 2-10. Cluster View

Use these areas as guides to ensure that the nets are fast/direct connect for implementation. Nets that connect within a rectangle can be implemented as fast/direct connects, depending on availability. For details about fast connects and direct connects, please see the *Actel FPGA Databook*.

Viewing Tiles

To view tiles:

1. **From the View menu, select *Static Objects* and click *RAM Tiles* or *Core Tiles*.** Borders appear around the RAM Tiles or Core Tiles, as shown in Figure 2-11.

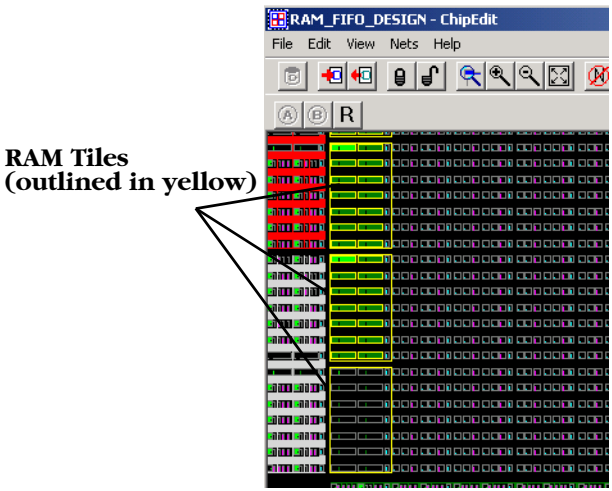


Figure 2-11. RAM Tiles

Use the Color Manager to customize the colors used to outline clusters and tiles. From the View Menu, click *Color Manager*.

Viewing I/O FIFO Blocks

To view I/O FIFO Blocks:

1. **From the View menu, select *Static Objects* and click *I/O FIFO Blocks*.** A colored border appears around the I/O FIFO Blocks.

Using ChipEdit with Other Tools

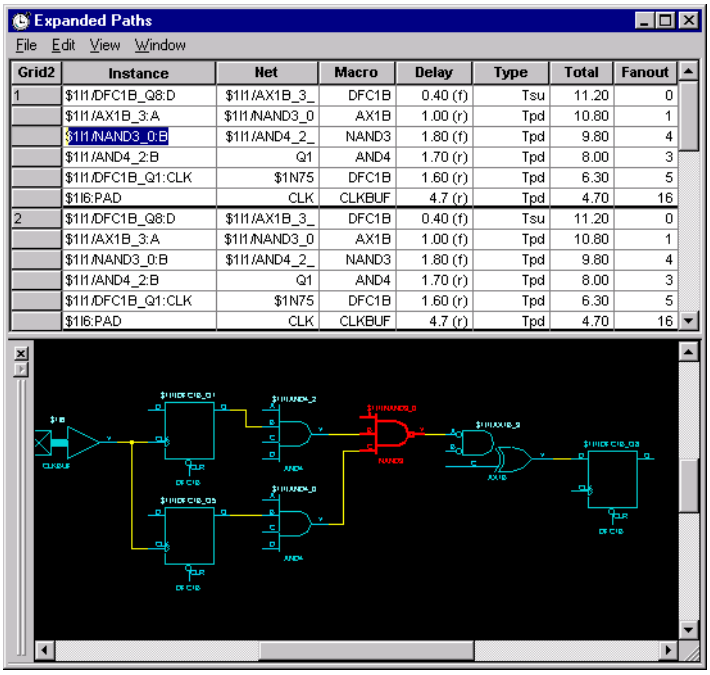
Using ChipEdit with Timer

Use ChipEdit and Timer together to view place-and-route of paths in ChipEdit.

To view paths:

1. **Open Timer and ChipEdit from Designer.**
2. **In Timer, click the *Paths* tab.**
3. **Select a Path set in the path set grid.** Paths within that set are displayed below in the path grid.
4. **Select the path you wish to expand.**
5. **Expand the path by double-clicking on the path, or in the Edit menu, click *Expand Path*.** The Expanded Paths window (Figure 2-12) opens and displays parallel paths in the Expanded Paths Grid and a

graphical representation of the paths in the Chart Window, as shown in Figure 2-12 on page 51.



Grid2	Instance	Net	Macro	Delay	Type	Total	Fanout
1	$1I1/DFC1B_Q8:D	$1I1/AX1B_3_	DFC1B	0.40 (f)	Tsu	11.20	0
	$1I1/AX1B_3:A	$1I1/NAND3_0	AX1B	1.00 (r)	Tpd	10.80	1
	$1I1/NAND3_0:B	$1I1/AND4_2_	NAND3	1.80 (f)	Tpd	9.80	4
	$1I1/AND4_2:B	Q1	AND4	1.70 (r)	Tpd	8.00	3
	$1I1/DFC1B_Q1:CLK	$1N75	DFC1B	1.60 (r)	Tpd	6.30	5
	$1I6:PAD	CLK	CLKBUF	4.7 (r)	Tpd	4.70	16
2	$1I1/DFC1B_Q8:D	$1I1/AX1B_3_	DFC1B	0.40 (f)	Tsu	11.20	0
	$1I1/AX1B_3:A	$1I1/NAND3_0	AX1B	1.00 (f)	Tpd	10.80	1
	$1I1/NAND3_0:B	$1I1/AND4_2_	NAND3	1.80 (f)	Tpd	9.80	4
	$1I1/AND4_2:B	Q1	AND4	1.70 (r)	Tpd	8.00	3
	$1I1/DFC1B_Q1:CLK	$1N75	DFC1B	1.60 (r)	Tpd	6.30	5
	$1I6:PAD	CLK	CLKBUF	4.7 (r)	Tpd	4.70	16

Figure 2-12. Timer Expanded Paths Window

The Expanded Paths grid shows all delay components for the selected path (Instance, Net, Macro, Delay, Type, Total Delay and Fanout details). For Delay, (r) stands for rising edge and (f) for falling edge.

Anything selected in the Expanded Paths grid or Graph window is reflected in both windows.

- Selecting the path number in the Expanded Paths grid highlights the entire path in the Chart window.
- Selecting an instance, net, or macro in the Expanded Paths grid highlights that selection in the Chart window.
- Selecting a logic macro in the Chart window, highlights all instances of the

macro in the Expanded Paths grid.

Toggle the Graph Window on and off by clicking *Graph Window* from the Window menu. Use the View command menu to Zoom in and out. In the Graph window, dragging the mouse downward and to the left will zoom fit. Dragging downward and to the right drags out a zoom in area.

Note: In some cases, long instance names may overlap and be difficult to read in the Graph window. This problem can be solved by moving the module. To move the module, select the module and while holding down the Shift key, click and drag the module to another location.

6. **Select a module or net in the Expanded Paths dialog box.** The module or net is shown in ChipEdit, as shown in Figure 2-13**.**

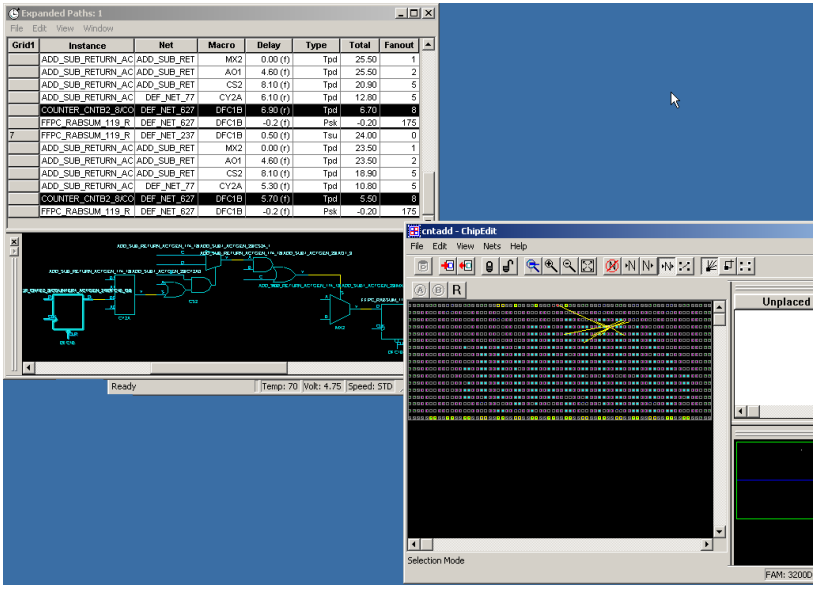


Figure 2-13. Timer and ChipEdit

Using ChipEdit with Silicon Explorer

Use ChipEdit to select probes for Silicon Explorer. To use ChipEdit with Silicon Explorer, you must have installed and be familiar with Silicon Explorer.

To select probes using ChipEdit:

1. **Open Silicon Explorer.**
2. **Load the probe file of the current design.**
3. **Start ChipEdit.**
4. **Synchronize data.** Click the R (Re-sync) button in ChipEdit's toolbar, as shown in Figure 2-14. When completed, the A and B buttons in the toolbar become activated.

Figure 2-14. ChipEdit's Silicon Explorer Toolbar

5. **Select a module in ChipEdit.**
6. **Click the *A* button in ChipEdit's toolbar to assign the selected module's output to probe A in Silicon Explorer.**
7. **Select another module in ChipEdit.**
8. **Click the *B* button in ChipEdit's toolbar to assign the selected module's output to probe B in Silicon Explorer.**
9. **From Silicon Explorer, click the *Acquire* toolbar button.** Waveforms are displayed in Silicon Explorer.

3 Using ChipView

ChipView only displays the results of place-and-route for ProASIC and ProASIC PLUS designs. Use ChipEdit for all other families. The results can be used to guide later place-and-route operations, if necessary. The ChipView creates no new data. It displays the design layout and is used for identifying problems and providing insights to solve them. The design shown in the ChipView is symbolic and does not reflect the actual ProASIC device resources. It shows relative placement positions and symbolic routes reflecting the congestion density of the layout. This section describes how to use the ChipView.

Note: Unlike ChipEdit, ChipView does not allow you to manually change placement.

Starting ChipView

ChipView, as shown in Figure 3-1, only supports the ProASIC and ProASIC PLUS families.

ChipView can only be started after you have placed and routed your design.

To access ChipView:

1. **After running Layout, click *ChipEdit* from Designer's Design Flow Window.**

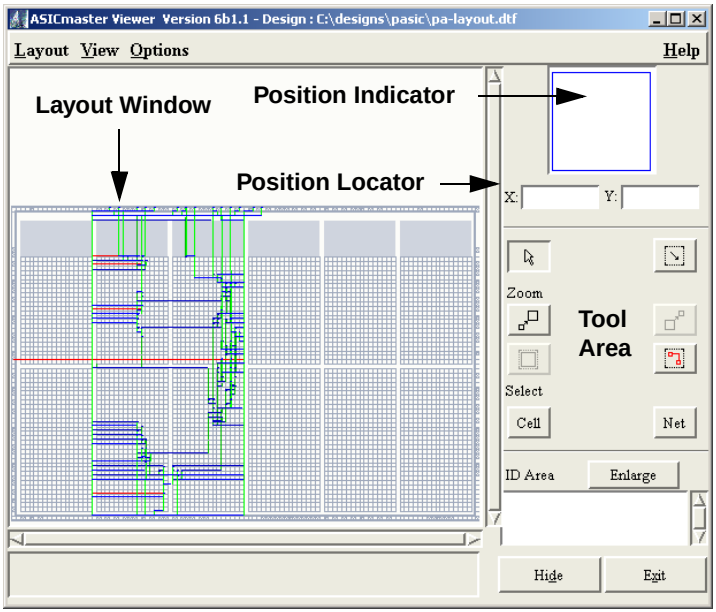


Figure 3-1. ProASIC Layout Viewer

Tool Area

ChipViewChipView Tool area, provides buttons for performing the operations described in the following sections.

Hide

Use the Hide button to enlarge the available layout display and hide the Tool area. To re-display the Tool area, select *Show Tool Area* from the Options menu.

Zoom In

Click the Zoom In button to magnify the design layout by a factor of 2.

Zoom Out

Clicking this button shrinks the design layout by a factor of 1/2.

Zoom Selected

Click this button to fit all selected objects into ChipView.

Zoom Area

Click this button to magnify a specific area in ChipView by clicking and dragging out the selected area.

Full View

Click the Full View button to fit the entire design into ChipView.

Pointer

The Pointer is used for object selection and is the default operation in the ChipView. If it is not active, click the Pointer button.

Information about selected objects is displayed in the ID Area. To select one object, click it. To select all objects in an area, click and drag across the objects you wish to select. Information about multiple selected objects is not automatically displayed in the ID area. To display the information, choose *Identify* from the View menu.

Cell

Click the Cell button to display the Select Cell by Name window, to search for and select cell by name. This is useful for selecting multiple cells.

Net

Click the Net button to display the Select Net by Name window, as shown in Figure 3-2, to search for and select nets by name.

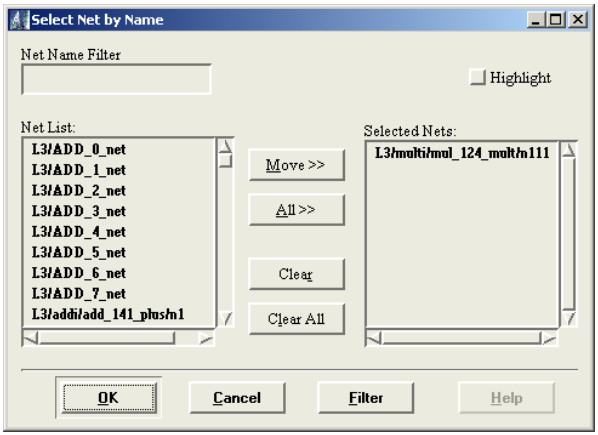


Figure 3-2. Select Net by Name window

The Select Net by Name window allows you to add or remove objects in the selected list and provides the following features:

- Net Name Filter text field supports the use of wildcard characters to filter out nets.
- Net List, a scroll list in which either all nets are displayed or a subset of nets are displayed when a filter is defined. Users can select nets they intend to highlight in the layout view.
- Selected Nets, a scroll list that contains all entries selected from the Net List area.
- Highlight button to provide a quick way to highlight all nets in the Selected Nets list.

The following buttons are located in the middle area of the Select Net by Name window.

- **Move** - Copies the selected entries in the Net List to Selected Nets.
- **All** - Copies all entries in the Net List to the Selected Nets list.
- **Clear** - Clears the selected items in the Selected Nets list.

- **Clear All** - Clears all entries in the Selected Nets list.

The following buttons are located at the bottom of the Select Net by Name window:

- **OK** - Confirms the selection process and closes the window.
- **Cancel** - Cancels the selection process.
- **Filter** - Starts the filter function.

Using the Filter Function

The Filter function performs a simple search. To perform the search, you must first specify a pattern. A pattern is a combination of strings and wildcard characters. The filter function accepts two commonly used wildcard characters:

- The question mark (?) matches exactly one single character.
- The asterisk (*) matches zero or more characters in sequence.

For example, if users want to search for all the internal nets of subcircuit L3/addu_1, enter the following in the Net Name text field:

```
L3/addu_1<Return>
```

Viewing Selected Nets

In some cases, such as a highly congested area, the number of nets displayed can be limited to only a few nets.

To view only selected nets:

1. **Select the nets you intend to examine using the Select Net by Name window or by dragging in the Layout area.**
2. **From the Options menu, Click *Show only Selected Nets*.** The layout window displays only the selected nets in the Layout area until the Show Only Selected Nets command is un-selected.

ID Area

The ID area displays information about an object when it is selected. When you select multiple objects, object information is not automatically displayed. To show information about all selected objects, choose the *Identify* command from the View menu.

Enlarging the ID Area

To enlarge the ID Area, click the Enlarge button, which opens a separate ID Area window. You can display ID information if the Tool area is hidden. The information displayed in the ID window is the same as that in the ID Area.

Position Indicator

The Position Indicator is located on the top right corner of the Tools area. The Position Indicator provides a quick way to move the viewer window to any position in a magnified layout.

Position Locator

The X and Y coordinate fields of the Position Locator display the current mouse position in ChipView. These are the X and Y coordinates of the tile where the cursor is placed. Their minimal values (1,1) are indicated in the lower-left corner of the ChipView window, and their maximum values, indicated in the top-right corner depend on the device that is targeted.

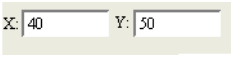


Figure 3-3. Position Locator

Highlighting Objects

You can highlight and unhighlight objects using the Highlight and Unhighlight commands in the View menu to identify them. For example, all objects in a subcircuit can be highlighted. The highlight color currently defined in the object setting is used. Different highlight colors can be used for different subcircuits. To unhighlight all selected objects, choose *Unhighlight All* in the View menu.

Customizing Design Layout Setup

The design layout in the ChipView window can be customized to assign new colors to objects and to control which objects are displayed using the Objects window.

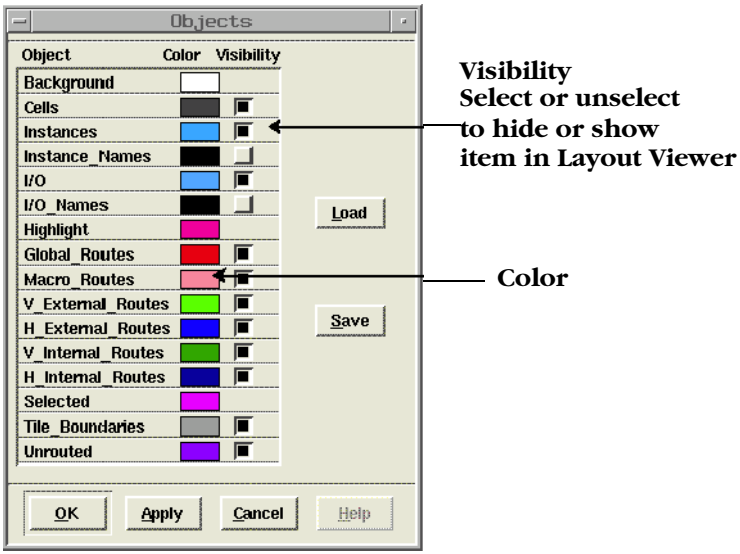


Figure 3-4. Objects Window

The Objects window displays the visibility status and colors of the different types of objects that appear in ChipView. Use the Objects window to modify an object's color and determine an object's visibility in the design layout. You can also save your customized object setup for later use. The Background, Highlight, and Selected objects do not have visibility controls because they are always visible.

The following buttons are located in the Objects window:

- **Color Control:** Displays the color chooser, with which you change an object's color.
- **Visibility:** Determines whether the associated object is visible in the design layout.

- **OK:** Confirms the object setup change process and closes the Objects window.
- **Apply**: Applies an object setup change and leaves the window open.
- **Cancel:** Cancels the object setup change and closes the window.
- **Load**: Displays a file browser to let you select the input file and then loads the current setup from the file you specified.
- **Save:** The first time you click *Save*, a file browser is displayed allowing you to specify the output file and save the current setup to the file you specified. Subsequent saves automatically save to the previously specified filename.

To customize ChipView window setup:

1. **From the Options menu, click *Objects*. This displays the Objects window.**
2. **Click an object's Color Control button to display the Color Chooser.**
3. **Pull down the Color Method menu to choose a color method. The methods are HLS, RGB, CMY, or Gray.**
4. **Change the object's color by using either the color wheel/plane or the color component values.**
5. **Click *OK*.**
6. **Set an object's visibility by toggling its Visibility check box.**
7. **Repeat steps 4-6 until all objects are set.**
8. **Click *Save*.**

Printing the Layout

To print the layout, choose *Print* from the Layout menu in the Design Layout window. The Design Layout uses the default printer for all printing. In UNIX, the PRINTER environment variable defines the default printer.

To change the printer setup:

1. **From the Layout menu, click *Printer*.** The printer window is displayed as shown in Figure 3-5.
2. **Specify the name of the printer to use.**

3. **Click *OK*.**

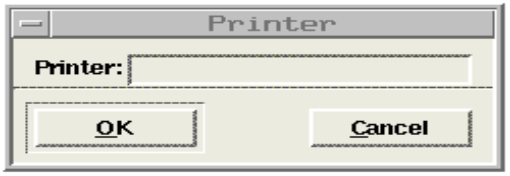


Figure 3-5. Printer Window

Exiting the Design Layout Window

The Design Layout window can be exited at any time by choosing Exit from the Layout menu. If you save the results of a run, you can display them again at any time.

Menu Commands

The following commands are available from ChipView.

The Layout Menu

Update: Updates the design layout. Useful when viewing the layout while placing/routing.

Print: Sends the Layout window to a PostScript printer. Uses the default printer (where $PRINTER points to) unless another printer is specified.

Printer: Displays the Printer window in which the user can specify a printer for subsequent Print commands.

Exit: Exits ChipView.

The View Menu

Highlight: Highlights a group of objects in colors other than the object colors defined in the objects window. Highlighting and Un-highlighting do not alter the current selection.

Unhighlight: Removes the highlight mark from all objects

Unhighlight All: Removes the highlight mark from all objects

Identify: Displays information about the selected objects in the ID area.

Zoom In: Magnifies the design layout around the center by a factor of 2.

Zoom Selected: Fits all selected objects into the Layout window.

Zoom Last Area: Magnifies a pre-defined area. Define this area by dragging a rectangle in the Layout window. This command is useful if you have a specific area you view often.

Full View: Fits the entire design into the Layout window.

Refresh: Redraws the Layout Window.

Select Cell by Name: Displays a window in which you can select cells by name. The command is useful if you want to select cells together.

Deselect All: Deselects all selected objects.

Options Menu

Object: Displays the Objects window where you can alter object colors and visibility flags.

Show Only Selected Nets: Toggle the Show Only Selected Nets flag. When the flag is set, the layout window only displays the selected nets. The command is useful if you want to view only one or two nets in a highly congested area.

Select: Changes the current pointer tool to Select, which selects objects in the Layout window.

Zoom Area: Changes the current pointer tool to Zoom Area, which highlights and magnifies an area you define by dragging out a rectangle in the Layout window. The Zoom Area command is also available in the Tool area.

Hide/Show Tool Area: Hides or shows the Tool area. If you need a larger Layout window, choose Hide Tool Area. A Hide button is also available in the Tool area.

A

Glossary

GTL+

Gunning Transceiver Logic Plus standard is a high speed bus standard (JESD 8.3). It requires a differential amplifier input buffer and an open drain output buffer. The output buffer requires switching between tristate and low. This is directly supported within the IO and the data does not have to be redirected through the output-enable path.

HSTL Class I

High-Speed Transceiver Logic standard is a general-purpose high speed 1.5V bus standard (EIA/JESD 8-6). It has four classes, of which we support Class I. It requires a differential amplifier input buffer and a push-pull output buffer.

LVCMOS 1.5V

LVCMOS for 1.5V is a projection of the LVCMOS standard for generalpurpose 1.5V applications. It uses a 3.3V tolerant CMOS input buffer and a push-pull output buffer.

LVCMOS 1.8V

LVCMOS for 1.8V is an extension of the LVCMOS standard (GESD 8.-5) used for general-purpose 1.8V applications. It uses a 3.3V tolerant CMOS input buffer and a push-pull output buffer.

LVCMOS 2.5V

Low-Voltage Complementary Metal-Oxide Semiconductor for 2.5V is an extension of the LVCMOS standard (GESD 8.-5) used for generalpurpose 2.5V applications. It uses a 3.3V tolerant CMOS input buffer and a push-pull output buffer.

LVDS

Low-Voltage Differential Signal is a moderate speed differential IO standard. It requires that one data bit is carried through two signal lines; therefore two pins are needed per input and output. It also requires an external resistor termination (e.g. ¼ component from Bourns CAT16- LV4F12). The voltage swing between these two signal lines is approximately 350mV. The AX family also contains dedicated circuitry supporting a high-speed LVDS standard.

LVPECL

Low-Voltage Positive Emitter Coupled Logic is another differential IO standard. It requires that one data bit is carried through two signal lines therefore two pins are needed per input and output. It also requires an external resistor termination (e.g. ¼ component from Bourns CAT16- PC4F12). The voltage swing between these two signal lines is approximately 850mV.

LVTTL

Low-Voltage Transistor-Transistor Logic is a general purpose standard (EIA/JESDSA) for 3.3V applications. It uses an LVTTL input buffer and push-pull output buffer.

PCI 3.3V

Peripheral Component Interface for 3.3V standard specifies support for both 33MHz and 66MHz PCI bus applications. It uses an LVTTL input buffer and a push-pull output buffer. The input and output buffers are 5V tolerant.

Ratsnest

The ratsnest view displays net connectivity between placed logic macros by connecting lines from the output pins to all input pins in the ChipView window.

SSTL3 Class I and II

Stub-Series Terminated Logic for 3.3V standard is a general-purpose 3.3V memory bus standard (JESD 8-8). It has two classes, of which we support both. It requires a differential amplifier input buffer and a pushpull output buffer.

SSTL2 Class I and II

SSTL for 2.5V standard is a general-purpose 2.5V memory bus standard (JESD 8-9). It has two classes, of which we support both. It requires a differential amplifier input buffer and a push-pull output buffer.

B

Product Support

Actel backs its products with various support services including Customer Service, a Customer Technical Support Center, a web site, an FTP site, electronic mail, and worldwide sales offices. This appendix contains information about contacting Actel and using these support services.

Actel U.S. Toll-Free Line

Use the Actel toll-free line to contact Actel for sales information, technical support, requests for literature, Customer Service, investor information, and using the Action Facts service.

The Actel toll-free line is (888) 99-ACTEL.

Customer Service

Contact Customer Service for non-technical product support, such as product pricing, product upgrades, update information, order status, and authorization.

From Northeast and North Central U.S.A., call (408) 522-4480.
From Southeast and Southwest U.S.A., call (408) 522-4480.
From South Central U.S.A., call (408) 522-4434.
From Northwest U.S.A., call (408) 522-4434.
From Canada, call (408) 522-4480.
From Europe, call (408) 522-4252 or +44 (0) 1276 401500.
From Japan, call (408) 522-4743.
From the rest of the world, call (408) 522-4743.
Fax, from anywhere in the world (408) 522-8044.

Actel Customer Technical Support Center

Actel staffs its Customer Technical Support Center with highly skilled engineers who can help answer your hardware, software, and design questions. The Customer Technical Support Center spends a great deal of time creating application notes and answers to FAQs. So, before you contact us, please visit our online resources. It is very likely we have already answered your questions.

Guru Automated Technical Support

Guru is a web-based automated technical support system accessible through the Actel home page (http://www.actel.com/guru/). Guru provides answers to technical questions about Actel products. Many answers include diagrams, illustrations, and links to other resources on the Actel web site.

Web Site

Actel has a World Wide Web home page where you can browse a variety of technical and non-technical information. The URL is http://www.actel.com.

Contacting the Customer Technical Support Center

Highly skilled engineers staff the Technical Support Center from 7:00 A.M. to 6:00 P.M., Pacific Time, Monday through Friday. Several ways of contacting the Center follow:

Electronic Mail

You can communicate your technical questions to our e-mail address and receive answers back by e-mail, fax, or phone. Also, if you have design problems, you can e-mail your design files to receive assistance. We constantly monitor the e-mail account throughout the day. When sending your request to us, please be sure to include your full name, company name, and your contact information for efficient processing of your request.

The technical support e-mail address is **tech@actel.com**.

Telephone

Our Technical Support Center answers all calls. The center retrieves information, such as your name, company name, phone number and your question, and then issues a case number. The Center then forwards the information to a queue where the first available application engineer receives the data and returns your call. The phone hours are from 7:00 A.M. to 6:00 P.M., Pacific Time, Monday through Friday. The Technical Support numbers are:

(408) 522-4460
(800) 262-1060

Customers needing assistance outside the US time zones can either contact technical support via email (tech@actel.com) or contact a local sales office. Please see our list of Worldwide Sales Offices.

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