SmartFusion2 SoC FPGA DSP FIR Filter Demo

User's Guide

Microsemi

Table of Contents

1 – SmartFusion2 SoC FPGA - DSP FIR Filter Demo

Introduction

SmartFusion®2 system-on-chip (SoC) field programmable gate array (FPGA) devices integrate a fourth generation flash-based FPGA fabric and an ARM® Cortex™-M3 processor. SmartFusion2 SoC FPGA fabric includes embedded mathblocks, which are optimized specifically for digital signal processing (DSP) applications such as, finite impulse response (FIR) filters, infinite impulse response (IIR) filters, and fast fourier transform (FFT) functions.

This demo shows a DSP FIR filter application using the SmartFusion2 device. In this DSP FIR filter application, the FIR filter is implemented in fabric for Low pass, High pass, Band pass, and Band reject filtering operations. The host interface is implemented in microcontroller subsystem (MSS) to communicate with the Host PC. A user friendly graphical user interface (GUI) generates the filter coefficients, input signals (Pass band frequency + stop band frequency) and also plots the input/output waveforms and the required spectrum. Microsemi CoreFIR filter IP is used to suppress the unwanted frequency components, and CoreFFT IP is used to generate the output spectrum to verify the filtering operation.

Figure 1-1 shows the top level diagram for DSP FIR filter demo.

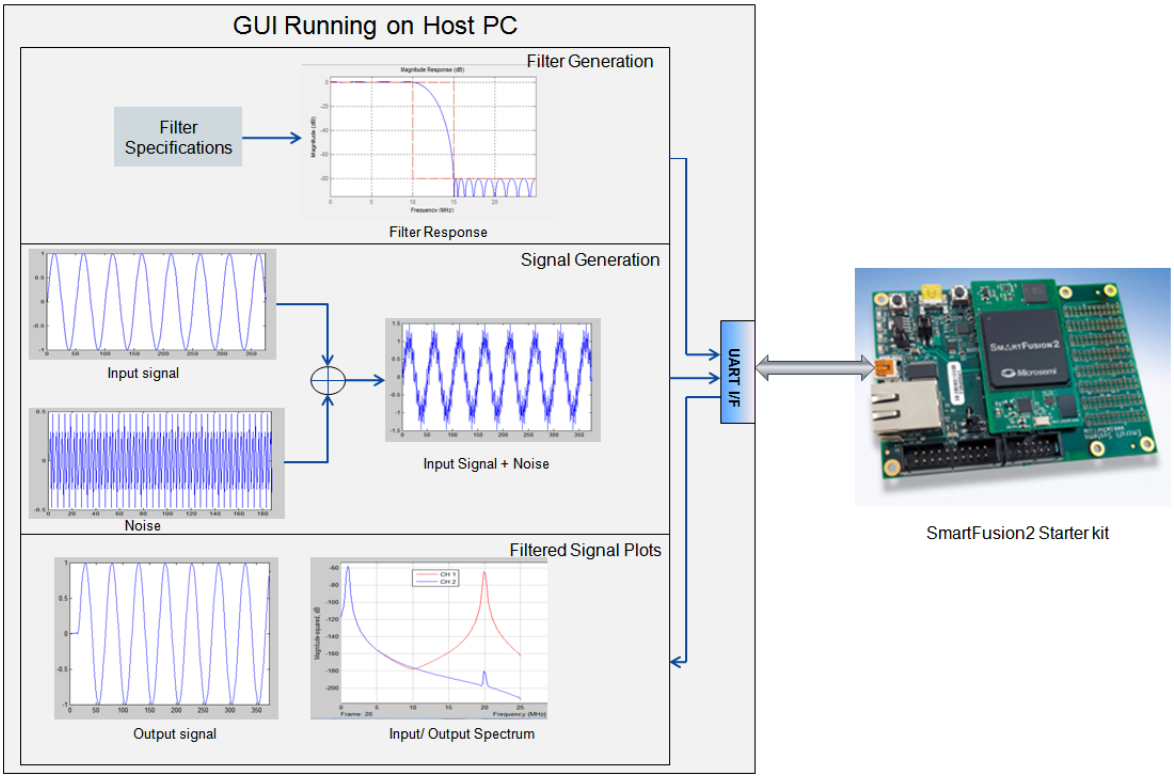

***Figure 1-1* • Top Level Diagram of DSP FIR Filter Demo**

Demo Requirements

This section explains the following:

- Hardware and software requirements
- Design files

Hardware and Software Requirements

The hardware and software required to run the demo are listed in Table 1-1.

***Table 1-1* • Required Hardware and Software to Run the Demo**

Hardware	**Version**
SmartFusion2 starter kit	SF2-STARTER-KIT-ES-2
FlashPro4 programmer	-
USB to Mini USB cable	-
Software	
FlashPro programming software	FlashPro - V 11.2
USB to UART drivers	-
Microsoft .NET framework 4 client for launching demo GUI	Version 4
Operating system	Windows XP SP2: 32-bit/64-bit Windows 7: 32-bit/64-bit

Demo Files

The files for this demo can be downloaded from the Microsemi website.

www.microsemi.com/soc/download/rsc/?f=FIR_FILTER_DEMO_DF

Demo file folder includes:

1. Programming file
2. GUI executable
3. Readme file

Refer to the Readme.txt file provided in the demo file folder for the complete directory structure.

Demo Design Description

This demo design is implemented using the following blocks:

- "MSS Block" (IPcore)
- "Control Logic" (user RTL)
- "TPSRAM IP" (IPcore)
- "CoreFIR" (IPcore)
- "CoreFFT" (IPcore)
- "SYSRESET"(IPcore)
- "OSC" (IPcore)
- "CCC" (IPcore)

Figure 1-2 on page 5 shows the detailed block diagram of the demo design.

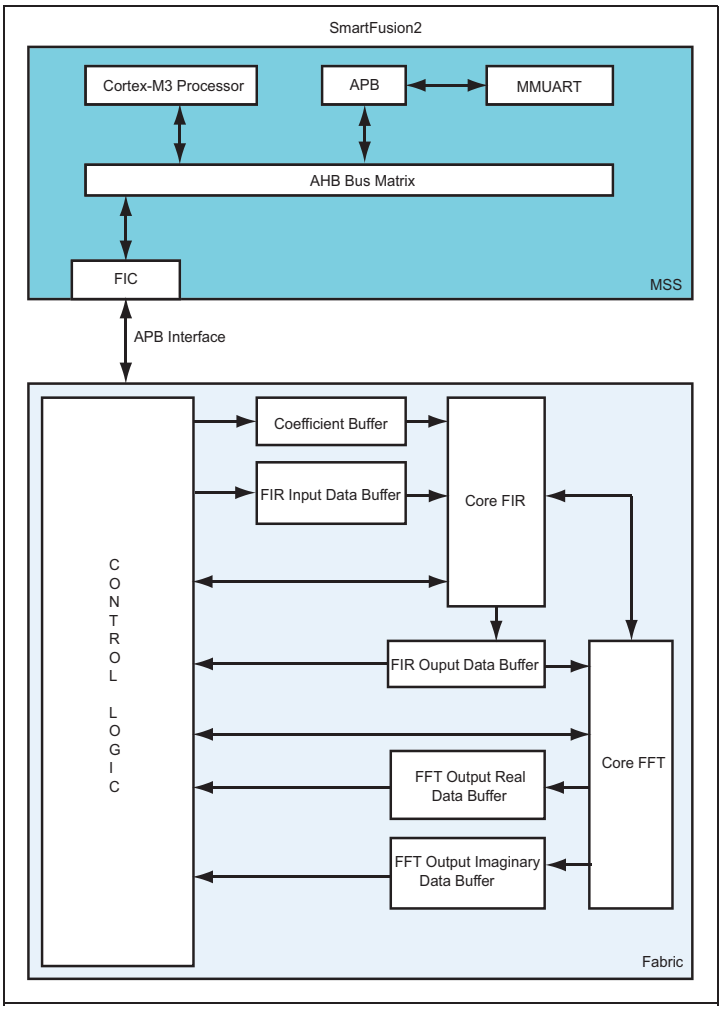

***Figure 1-2* • DSP FIR Filter Demo Block Diagram**

MSS Block

MSS block sends and receives the data between host PC (GUI interface) and fabric logic. MMUART interface is used to communicate with the host PC. FIC_0 interface (APB master) is used to communicate with the fabric user logic.

Control Logic

This is the user logic implemented in the fabric and consists of the following two finite-state machine (FSM)s:

- **Data Handling**: Implements and controls operations like loading the filter input data to the corresponding input data buffer and loading filter coefficients to the corresponding coefficient memory buffers. An APB bus slave is implemented to communicate with the MSS APB master.
- **Filter Control**: Controls the FIR filter and FFT operations. Loads the filtered data to corresponding output buffer and moves the FFT output data to the corresponding output data buffer.

TPSRAM IP

TPSRAM IP is used to implement the following:

- Filter coefficient buffer (depth: 63, width: 16)
- Input signal data buffer (depth: 1024, width: 16)
- Output signal buffer (depth: 1024, width: 16)
- Output signal FFT real data buffer (depth: 1024, width: 16)
- Output signal FFT imaginary data buffer (depth: 1024, width: 16)

CoreFIR

The Core FIR IP is used in Reloadable coefficient mode to support Low pass, High pass, Band pass, and Band reject filters. Core FIR IP configuration is as follows:

- Version: 8.4.101
- Filter Type: Single rate fully enumerated
- No of taps: 63
- Coefficients type: Reloadable
- Coefficients bit width: 16(signed)
- Data bit width: 16 (signed)
- Filter structure: Transposed with symmetry

CoreFFT

The Core FFT IP is used for generating the frequency spectrum of the filtered data. Core FFT IP configuration is as follows:

- Version: 6.3.102
- FFT Architecture: In place
- FFT type: Forward
- FFT Scaling: Conditional
- FFT Transform Size: 256
- Width: 16

SYSRESET

SYSRESET IP provides the power on reset signal.

OSC

OSC IP is configured as an RC oscillator to provide the 50 MHz signal to the CCC (Clock conditioning circuit)

CCC

CCC IP is configured to provide a 100 MHz clock signal

For detailed smart design implementation and resource usage summary refer to "Smart Design Implementation".

Demo Flow

Demo Setup

1. As shown in Figure 1-3, connect the FlashPro 4 programmer to the FlashPro header on the SmarFusion2 starter kit.
2. Connect one end of the USB mini-B cable to the respective USB connector provided on the SmartFusion2 starter kit.

Figure 1-3 shows the board setup for running the DSP FIR filter demo on the SmartFusion2 starter kit.

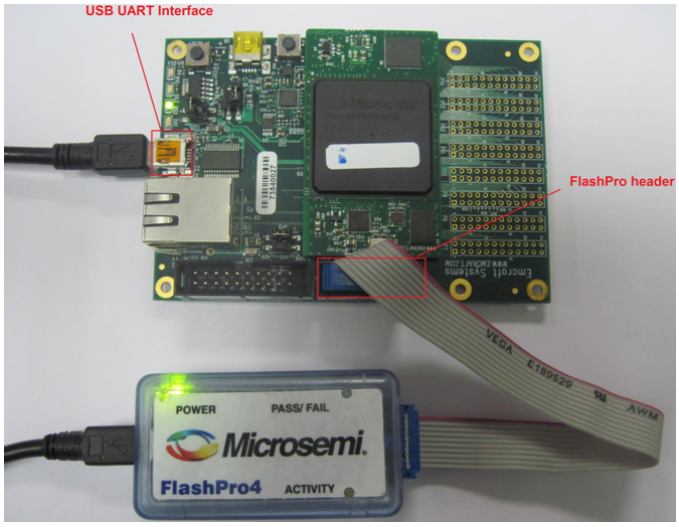

***Figure 1-3* • SmartFusion2 SoC FPGA Starter Kit Setup**

3. Connect the other end of the USB cable to the host PC. Make sure that the USB to UART bridge drivers are automatically detected (can be verified in the Device Manager), as shown in Figure 1-4.

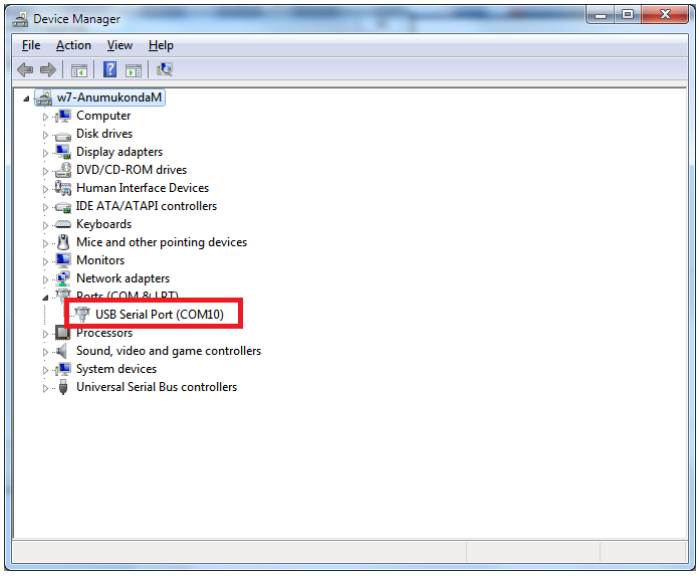

***Figure 1-4* • USB to UART Bridge Drivers**

4. If USB to UART bridge drivers are not installed, download and install the drivers from www.microsemi.com/soc/documents/CDM_2.08.24_WHQL_Certified.zip.
5. Jumper settings can be left as Default Settings.

DSP FIR Demo GUI

DSP FIR demo is provided with a user friendly GUI that runs on the host PC to communicate with SmartFusion2 starter kit. UART is used as the underlying communication protocol between the host PC and SmartFusion2 starter kit. Figure 1-5 shows the DSP FIR demo GUI.

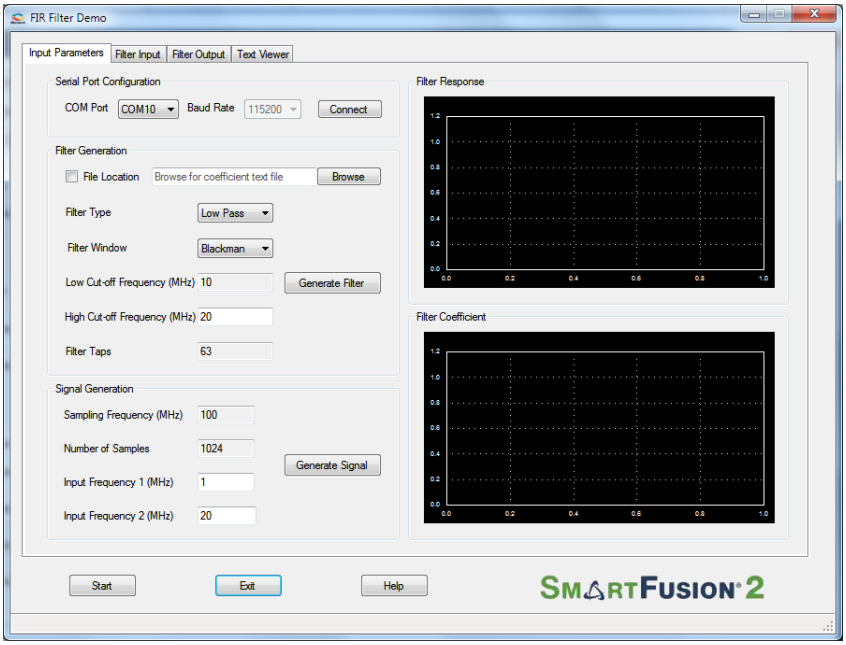

***Figure 1-5* • DSP FIR Demo GUI**

The DSP FIR demo GUI consists of the following tabs:

- **Input Parameters**: Configures the serial COM port, filter generation, and signal generation.
- **Filter Input**: Plots input signal and its frequency spectrum
- **Filter Output**: Plots output signal and its frequency spectrum
- **Text Viewer**: Shows coefficients, input signal, output signal, and FFT data values

Click **Help** for more information on the GUI as shown in Figure 1-6.

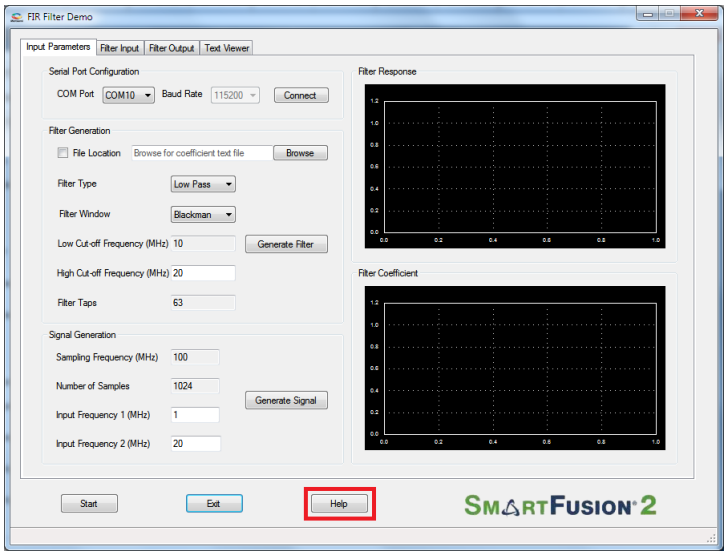

***Figure 1-6* • DSP FIR Demo GUI Help**

Running the Demo

1. Program the SmartFusion2 device with the programming file provided in the design files (\\FILTER_FIR_DEMO\Programming File\ FILTER_FIR_DEMO.stp) using the FlashPro design software.
2. Launch the DSP FIR Demo GUI executable file available in the design files. (\\FILTER_FIR_DEMO\GUI\SF2_FIR_Filter.exe). The GUI window is displayed, as shown in Figure 1-7.

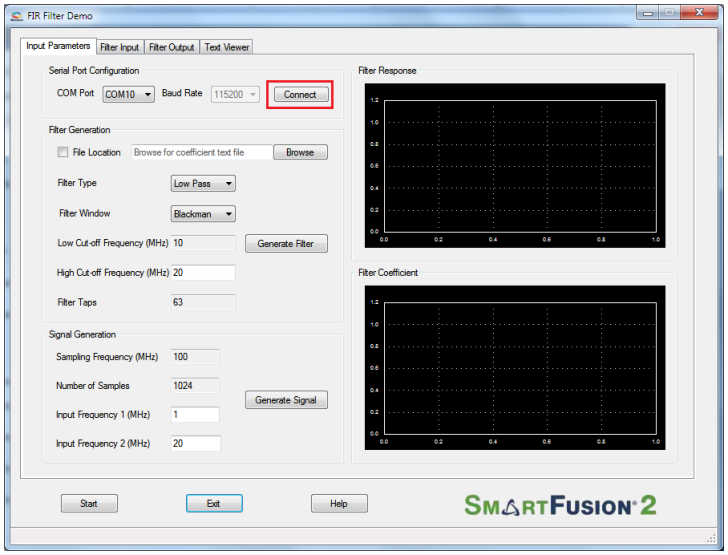

***Figure 1-7* • Serial Port Configuration**

3. **Serial Port Configuration**: The COM port number is automatically detected and baud rate is fixed at 11, 5200. Press **Connect** as shown in Figure 1-7.

4. **Filter Generation**: Two options are provided for generating the filter coefficients:

   1. Generate the coefficients using MATLAB or any similar tool and save it as a text file (Refer "Coefficient Text File Format" for the format of the text file). The GUI can be used to browse and load this file as shown in Figure 1-8.

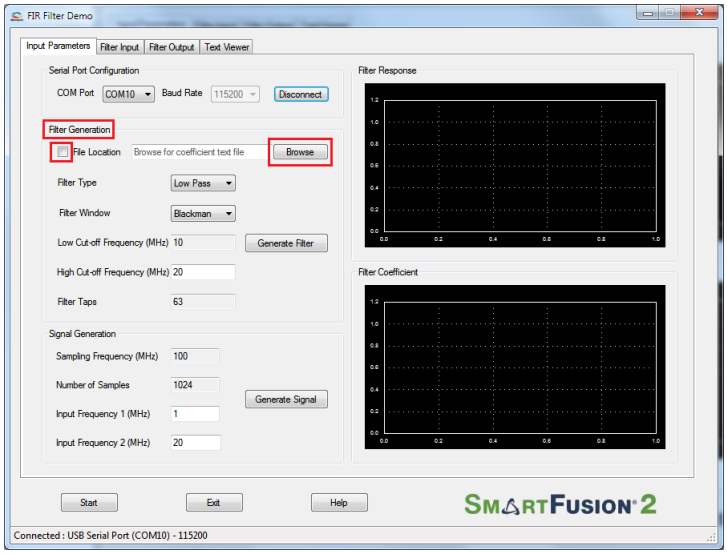

Figure 1-8 • **Filter Generation - 1**

2. Generate the Filter coefficients using GUI as given below:

As shown in Figure 1-9 the following parameters are required to generate filter coefficients.

- **Filter Type**: Low Pass (Low Pass/High Pass /Band Pass/Band Reject filter)
- **Filter Window**: Blackman (Blackman/Hamming window)
- **Low Cut-off Frequency**: Disabled for Low Pass filter required (High cut-off frequency is disabled for High pass filter)
- **High Cut-off Frequency**: 20 MHz
- **Filter Taps**: 63 (Fixed)

Press **Generate Filter** to generate the filter coefficients.

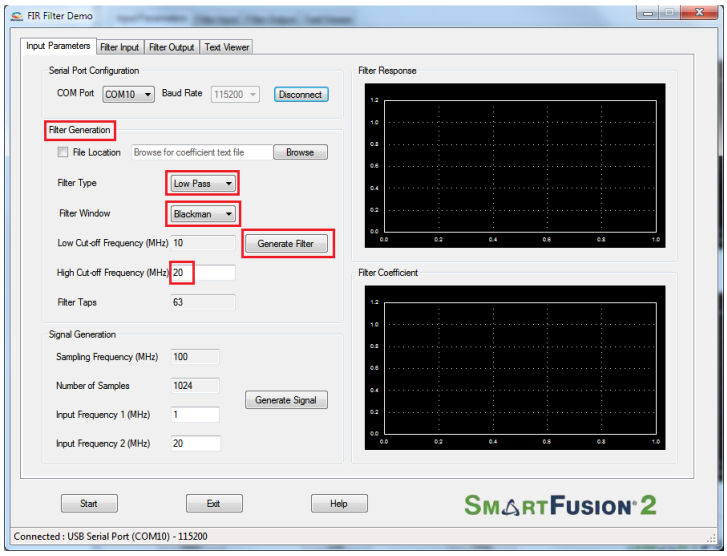

***Figure 1-9* • Filter Generation - 2**

5. After successful generation of the filter coefficients, filter response and the filter coefficient plots (graphs) are displayed as shown in Figure 1-10.

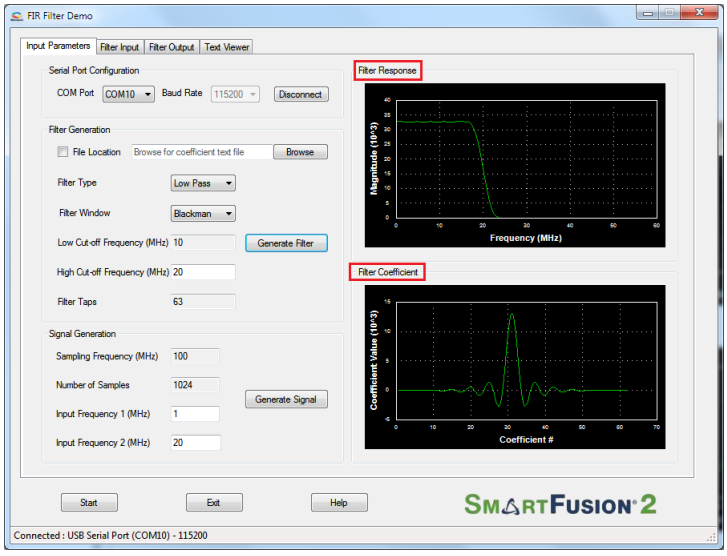

***Figure 1-10* • Filter Response and Filter Coefficient Plot**

6. Signal Generation:
   - **Sampling Frequency**: 100 MHz (Fixed)
   - **Number of Samples**: 1024 (Fixed)
   - **Input Frequency 1**: Enter the signal frequency in the pass band region, For example, 1MHz to High cut-off frequency
   - **Input Frequency 2**: Enter the signal frequency in the stop band region.For example, High cut-off frequency to Sampling frequency /2

   Click **Generate Signal** as shown in Figure 1-11.

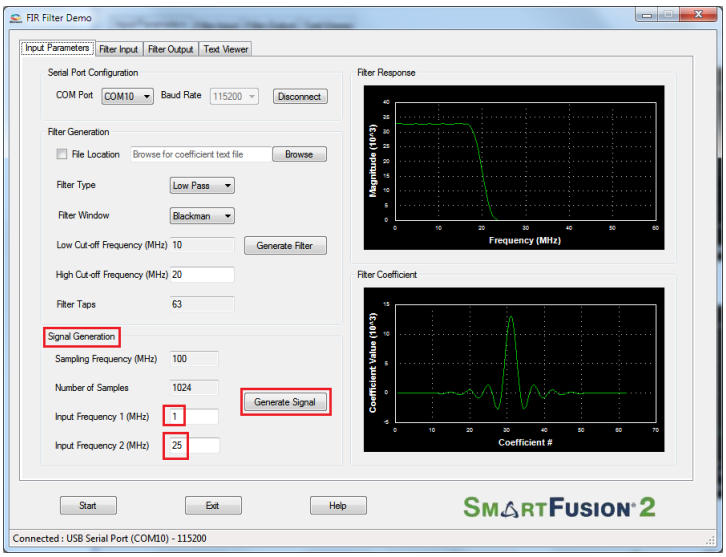

***Figure 1-11* • Signal Generation**

7. Input signal and the frequency spectrum of the specified signal are displayed as shown in Figure 1-12.

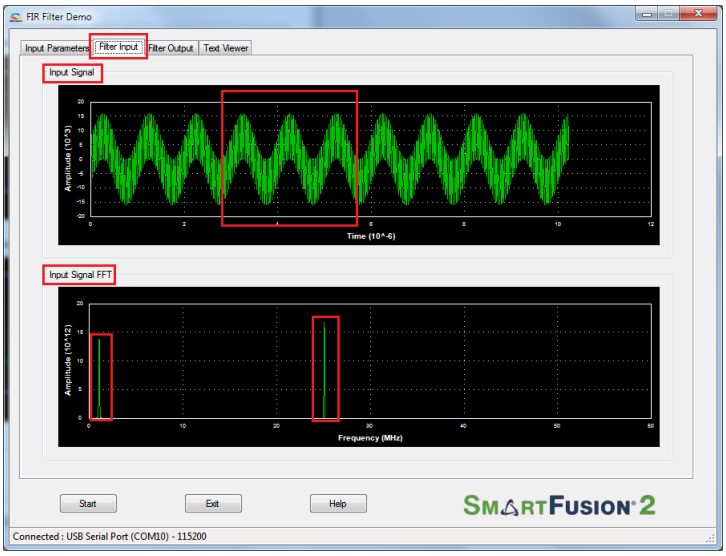

***Figure 1-12* • Input Signal and Input Signal FFT Plot**

8. The input frequencies and coefficients can be configured by clicking on **Start** as shown in Figure 1-13. It sends the input data (1 k samples) and filter coefficients to the SmartFusion2 device for processing the filtering operation.

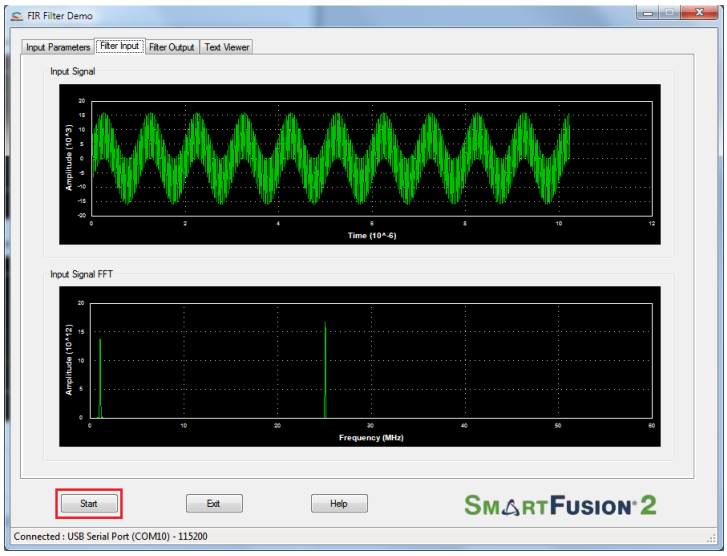

***Figure 1-13* • DSP FIR Filter Demo Start**

9. After completing the filter operation by SmartFusion2, the GUI plots the filtered data and FFT data on filter output window as shown in Figure 1-14. Since Low pass filter option was selected, the High frequency component is suppressed while the Low frequency signal is preserved. This can be observed in the frequency spectrum of the output signal.

***Figure 1-14* • Filtered Signal: Time and Frequency Plot**

10. Right-click on the window, it shows different options as shown in Figure 1-15. The data can be copied, saved, and exported to CSV plot for analysis purpose. Page setup, print, show point values, zoom, and set scale are set to default.

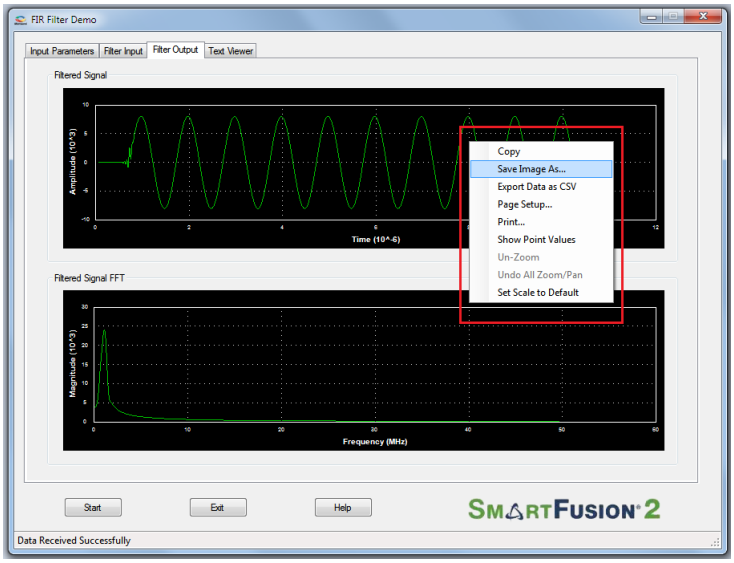

***Figure 1-15* • Filtered Signal: GUI options**

11. The filter coefficients, input signal, output signal, and FFT output data values can be viewed in Text viewer. Click on **Text Viewer** tab and then click on the corresponding **View** button as shown in Figure 1-16.

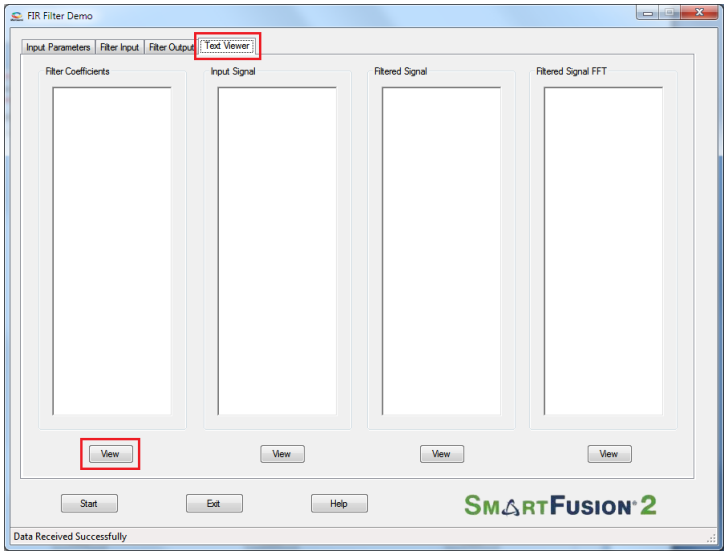

***Figure 1-16* • Text Viewer**

12. The values can be observed as shown in Figure 1-17.

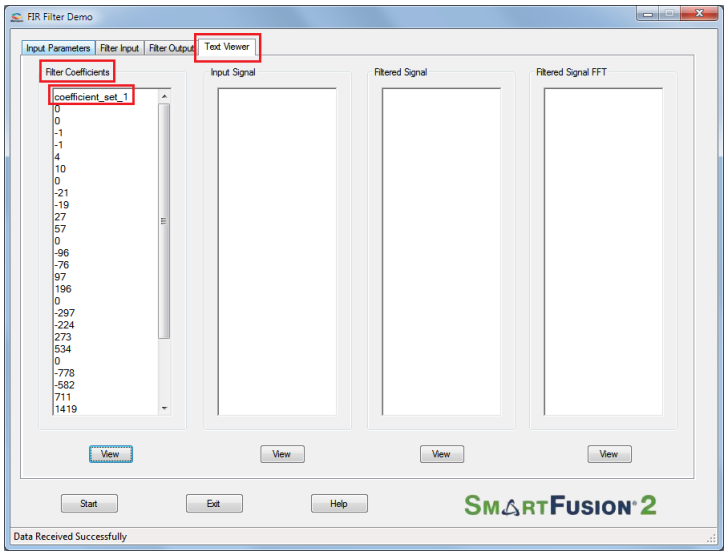

***Figure 1-17* • Text Viewer: Filter Coefficient Values**

13. To save the coefficients as a text file, right-click on the filter Coefficients window, it shows different options as shown in Figure 1-18. Now click on **Save.** Select OK to save the text file.

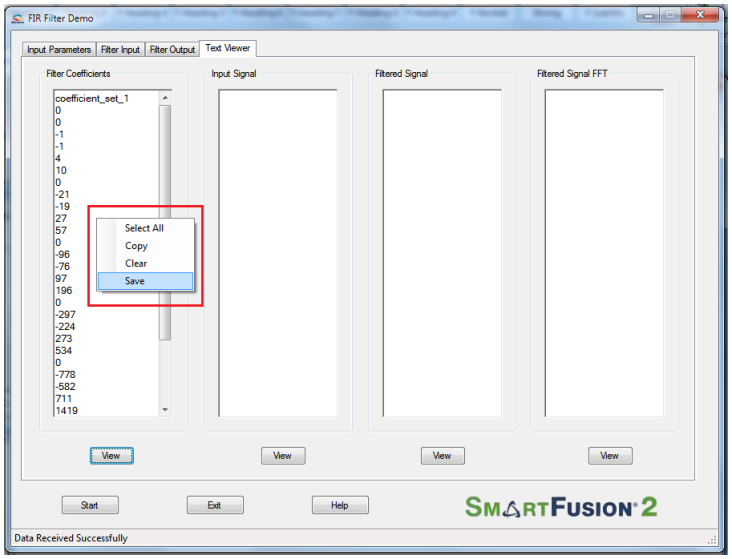

***Figure 1-18* • Text Viewer: Coefficients Save Options**

14. Click **Exit** to stop the demo as shown in Figure 1-19.

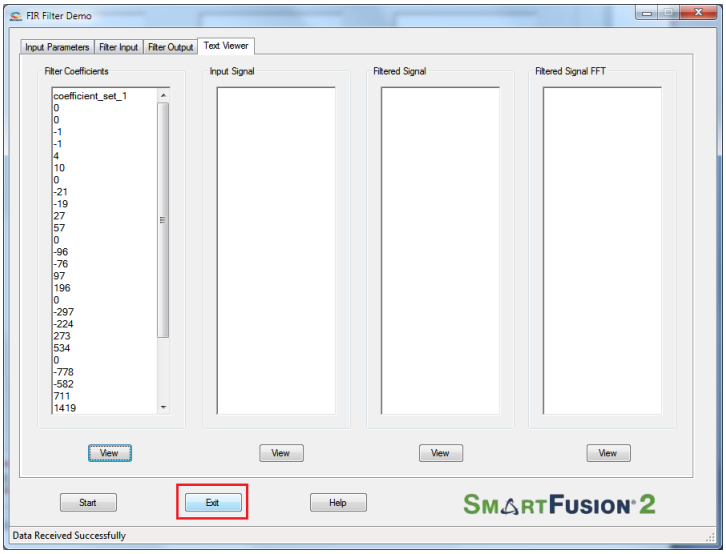

***Figure 1-19* • Exit Demo**

Conclusion

This demo shows the features of the SmartFusion2 device including MSS, Mathblocks, and LSRAMS for DSP specific applications. Also provides information about how to use the Microsemi DSP IP cores (CoreFIR, CoreFFT). This GUI based demo is very easy to use and provides many options to understand and implement DSP filters on the SmartFusion2 device.

A – Smart Design Implementation

Smart Design Implementation

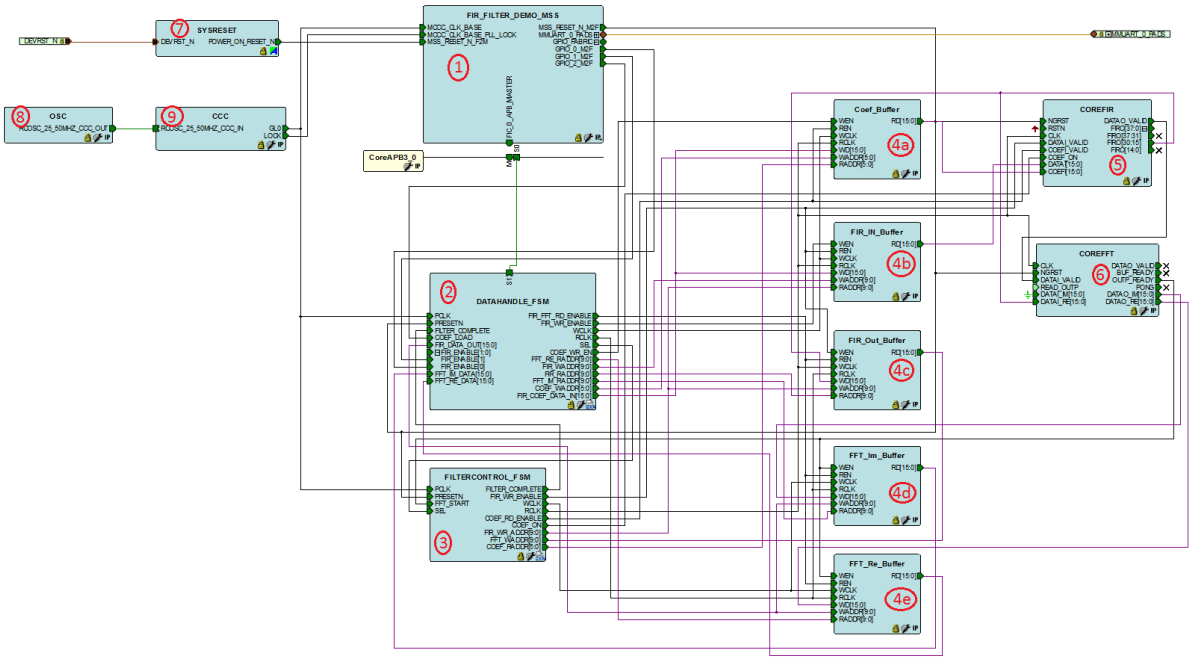

***Figure A-1* • DSP FIR Filter Smart Design**

***Table A-1* • DSP FIR Filter Demo Smart Design Blocks and Description**

S.No	Block Name	Description
1	FIR_FILTER_DEMO_MSS	The MSS block that is configured to handle communication between the host PC and fabric logic.
2	DATAHANDLE_FSM	Control logic to send/receive the data between MSS and data buffers.
3	FILTERCONTROL_FSM	Control logic to generate the control signals for FIR and FFT operations.
4	Coef_Buffer	TPSRAM IP for filter coefficient buffer
	FIR_IN_Buffer	TPSRAM IP for FIR input signal data buffer
	FIR_Out_Buffer	TPSRAM IP for FIR output signal buffer
	FFT_Im_Buffer	TPSRAM IP for FFT output imaginary data buffer
	FFT_Re_Buffer	TPSRAM IP for FFT output real data buffer
5	COREFIR	COREFIR IP
6	COREFFT	COREFFT IP
7	SYSRESET	Reset IP

***Table A-1* • DSP FIR Filter Demo Smart Design Blocks and Description (continued)**

S.No	Block Name	Description
8	OSC	Oscillator IP
9	CCC	Clock Conditioning circuit IP

Resource Usage Summary

Device: SmartFusion2 device

Die: M2S050T_ES

Package: 896 FBGA

***Table A-2* • DSP FIR Filter Demo Resource Usage Summary**

Type	Used	Total	Percentage
COMB	1814	56340	3.22
SEQ	3094	56340	5.49
RAM64x18	0	72	0.00
RAM1Kx18	12	69	17.39
MACC	36	72	50.00

***Table A-3* • MACC Blocks Usage Summary**

CoreFIR	CoreFFT	Total
32	04	36

***Table A-4* • RAM1Kx18 Blocks Usage Summary**

CoreFIR	CoreFFT	Fabric Buffers	Total
0	7	5	12

B – Coefficient Text File Format

Coefficient Text File Format

The FIR filter coefficients can be loaded from an ASCII text file (* .txt). Create the coefficient file using a text editor. The format of text file should be as shown in Figure B-1. Coefficient values must be entered as integer numbers. For a symmetric or anti-symmetric filter, only half of the coefficients must be listed in the file (applies to the Fully Enumerated type only). Only one coefficient value per line is permitted. An extra empty line must be placed after the last coefficient of the last set.

```
coefficient_set_1
5
6
10
25
63
- 1
- 11
- 32
- 63
```

***Figure B-1* • Coefficient File Example - 9 Taps, Decimal Values**

C – List of Changes

The following table lists critical changes that were made in each revision of the chapter in the demo guide.

Date	Changes	Page
Revision 1 (November 2013)	Updated the document for Libero v11.2 software release (SAR 52985).	NA
Revision 0 (April 2013)	Initial release	NA

D – Product Support

Microsemi SoC Products Group backs its products with various support services, including Customer Service, Customer Technical Support Center, a website, electronic mail, and worldwide sales offices. This appendix contains information about contacting Microsemi SoC Products Group and using these support services.

Customer Service

Contact Customer Service for non-technical product support, such as product pricing, product upgrades, update information, order status, and authorization.

From North America, call 800.262.1060
From the rest of the world, call 650.318.4460
Fax, from anywhere in the world, 408.643.6913

Customer Technical Support Center

Microsemi SoC Products Group staffs its Customer Technical Support Center with highly skilled engineers who can help answer your hardware, software, and design questions about Microsemi SoC Products. The Customer Technical Support Center spends a great deal of time creating application notes, answers to common design cycle questions, documentation of known issues, and various FAQs. So, before you contact us, please visit our online resources. It is very likely we have already answered your questions.

Technical Support

Visit the Customer Support website (www.microsemi.com/soc/support/search/default.aspx) for more information and support. Many answers available on the searchable web resource include diagrams, illustrations, and links to other resources on the website.

Website

You can browse a variety of technical and non-technical information on the SoC home page, at www.microsemi.com/soc.

Contacting the Customer Technical Support Center

Highly skilled engineers staff the Technical Support Center. The Technical Support Center can be contacted by email or through the Microsemi SoC Products Group website.

Email

You can communicate your technical questions to our email address and receive answers back by email, fax, or phone. Also, if you have design problems, you can email your design files to receive assistance. We constantly monitor the email account throughout the day. When sending your request to us, please be sure to include your full name, company name, and your contact information for efficient processing of your request.

The technical support email address is soc_tech@microsemi.com.

My Cases

Microsemi SoC Products Group customers may submit and track technical cases online by going to My Cases.

Outside the U.S.

Customers needing assistance outside the US time zones can either contact technical support via email (soc_tech@microsemi.com) or contact a local sales office. Sales office listings can be found at www.microsemi.com/soc/company/contact/default.aspx.

ITAR Technical Support

For technical support on RH and RT FPGAs that are regulated by International Traffic in Arms Regulations (ITAR), contact us via soc_tech_itar@microsemi.com. Alternatively, within My Cases, select **Yes** in the ITAR drop-down list. For a complete list of ITAR-regulated Microsemi FPGAs, visit the ITAR web page.

Microsemi Corporate Headquarters
One Enterprise, Aliso Viejo CA 92656 USA
Within the USA: +1 (949) 380-6100
Sales: +1 (949) 380-6136
Fax: +1 (949) 215-4996

Microsemi Corporation (NASDAQ: MSCC) offers a comprehensive portfolio of semiconductor solutions for: aerospace, defense and security; enterprise and communications; and industrial and alternative energy markets. Products include high-performance, high-reliability analog and RF devices, mixed signal and RF integrated circuits, customizable SoCs, FPGAs, and complete subsystems. Microsemi is headquartered in Aliso Viejo, Calif. Learn more at **www.microsemi.com**.

© 2013 Microsemi Corporation. All rights reserved. Microsemi and the Microsemi logo are trademarks of Microsemi Corporation. All other trademarks and service marks are the property of their respective owners.

50200438-1/11.13