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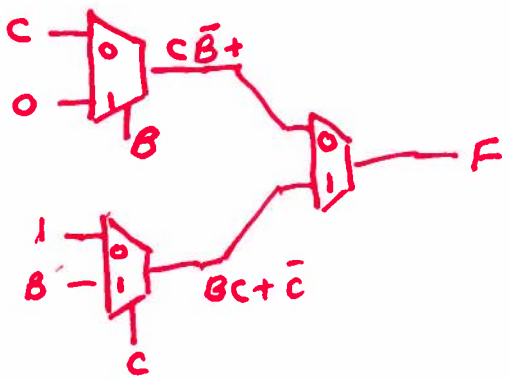
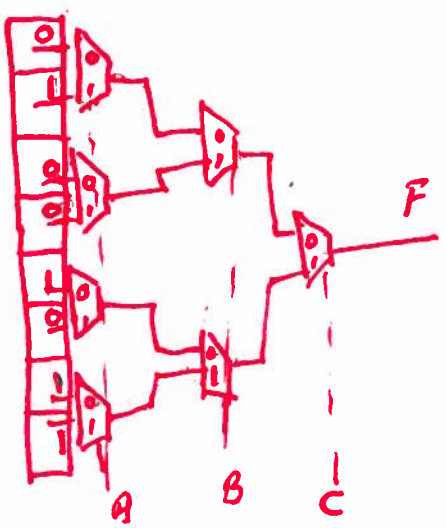
Q1

$$F = AB\bar{C} + A\bar{B}\bar{C} + ABC + \bar{A}\bar{B}C$$
$$= A\bar{C} + ABC + \bar{A}\bar{B}C$$
$$= A(BC+\bar{C}) + \bar{A}\bar{B}C$$



A	B	C	F
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	1



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Q2

N unsigned $\geq 4 \geq 0$ ∴ Possible values : 0, 1, 2, 3, 4.

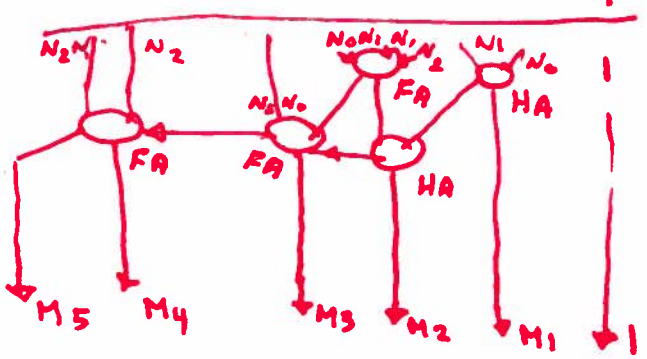
Therefore 3-bits is sufficient to represent $N = N_2 N_1 N_0$

$N_2 N_1 N_0$
$N_2 N_1 N_0$

N_0N_2 N_0N_1 N_0N_0
N_1N_2 N_1N_1 N_1N_0
N_2N_2 N_2N_1 N_2N_0

N_2N_1 N_2N_0 N_1N_0 0 N_0
N_2 N_1

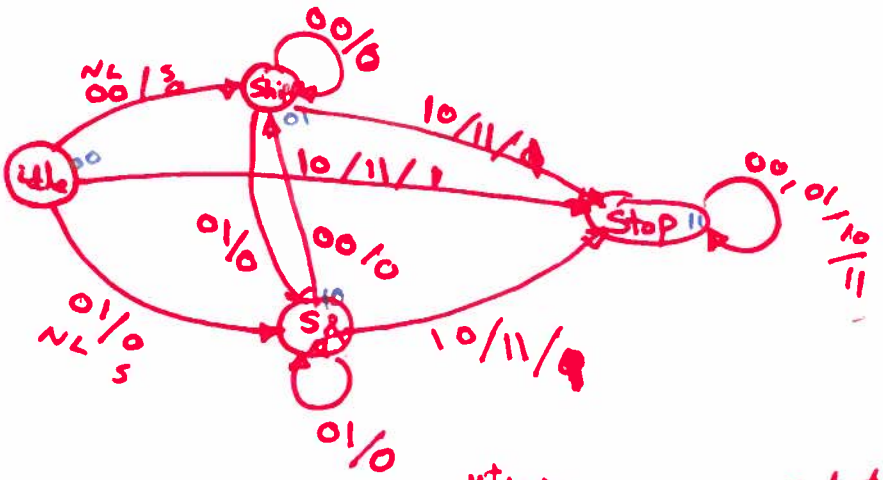
N_2 N_1 N_0 + N
1 + 1



Total Area = 3FA + 2HA

Delay = AND_{delay} + $2FA_{delay}$ + $2HA_{delay}$

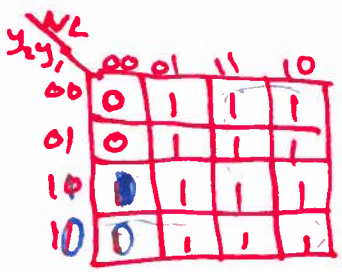
Q3 COEN 6501 DEC 2014



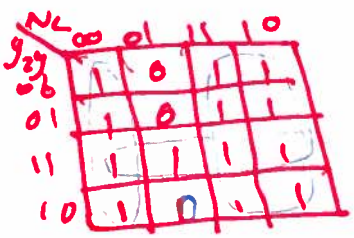
State Assignment

idle	00
Shift	01
Shift&Add	10
Stop	11

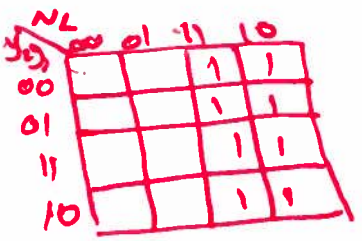
y_2y_1	$y_2^+y_1^+$ 00	01	11	10	output, S 00	01	11	10
00	01	10	11	11	0	0	1	1
01	01	10	11	11	0	0	1	1
11	11	11	11	11	0	0	1	1
10	01	10	11	11	0	0	1	1



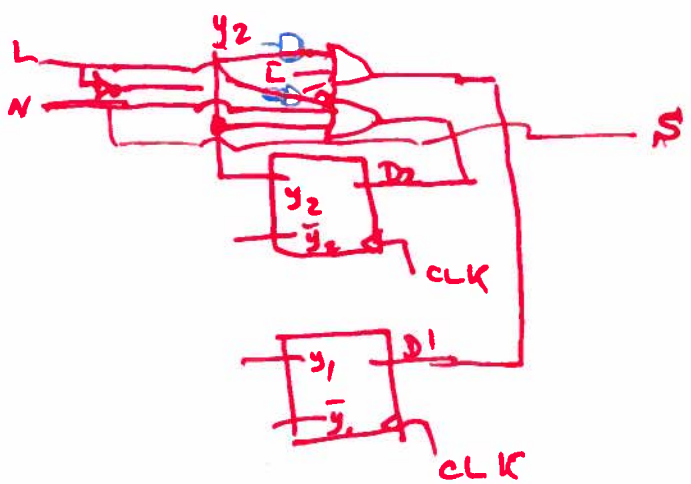
$Y_2^+ = y_2y_1 + N\bar{L} + \bar{L}$



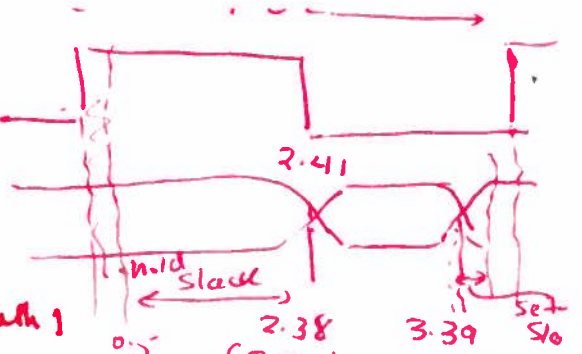
$Y_1 = y_2y_1 + N + \bar{L}\bar{N}$



$S = N$



Q4) COEN 650 Dec 2014



a) All the paths

(3)

$U_2 \cdot U_{10}\ U_{11}$	Path 1
$U_2\ U_3\ U_6\ U_7\ U_8$	Path 2 ←
$U_8\ U_9\ U_{10}\ U_{11}$	Path 3
$U_8\ U_1\ U_2$	Path 4
$U_8\ U_6\ U_7\ U_8$	Path 5
$U_8\ U_5\ U_7\ U_8$	Path 6 ← This is the critical path 3.96
$U_{11}\ U_{10}\ U_{11}$	Path 7
$U_{11}\ U_4\ U_1\ U_2$	Path 8
$U_{11}\ U_4\ U_5\ U_7\ U_8$	Path 9 ←

b) Paths to be analyzed are Path 2 and Path 9 as others are within the same range

(4)

Path 2 C_L = $0.1(1.5+1)+0.2(2)+0.1(2)+0.08(1)+0.15+0.05(2)+0.14(1)+0.24$
$+0.05(2)+0.14(1)+0.24 = 2.09$

Path 9 C_L = $0.1(1.5+1)+0.2(2)+0.1(2+2)+0.08(2)+0.15+0.05(2)+0.14(1)+0.24$
$+0.05(2)+0.14(1)+0.24 = 2.32$ ←

Path 9 is selected but Paths 6 and Path 3 almost equal.

$T_{Max} = T_{CQ} + T_{CL} + T_{SU} = 1.5 + 2.32 + 1 = 4.82$ ns

Frequency = $\frac{10^9}{4.82} = 207$ MHz

c) Set-up

(3)

Slack time = $t_{required} - t_{arrival} - t_{set\,up}$

Critical for U_2 is path 8

$T_{CL} = 1.5 + 0.1(1+2) + 0.2(2) + 0.15 + 0.1(2+2) + 0.08(2) + 0.24 + 0.05(2) + 0.14 = 3.$

set-up slack = $4.82 - 3.39 - 1 = 0.43$ ns → 0.57

Hold-time slack time

$T_{hold} < t_{CQmin} + C_{L\,min} - t_{hold}$

Path 4 is the shortest path $U_8 - U_1 - U_2$

$T_{CLmin} = 1.5 + 0.1(2) + 0.2(1) + 0.24 + 0.5(2) + 0.14(1) = 2.38$

$t_{hold\ slack} <$ 2.38

Q5 CSEN 6501 DEC 2014

a) Arrival time @ point B

$T_{arrival\ B} = 2 + 0.45(1+2+3) + 0.4 + 0.35*(4)$
$= 6.5$ ns

$T_{arrival\ C} = 2 + 0.45(1+2+3) + 0.2 + 0.15(4)$
$= 5.5$ ns

Required Time @ B $= T - t_{setup} = 20 - 1 = 19$ nsec

" " @ C $= T - t_{setup} + t_{skew} = 20 - 1 + 2 = 21$ n sec

Slack @ B $= 19 - 6.5 = 12.5$ n sec

" " C $= 21 - 5.5 = 15.5$ n sec

	Arrival	Required	Slack
B	6.5	19	12.5
C	5.5	21	15.5

b) There are 5 paths of which D2 → U3 → D1 is critical

$T_C = \underline{0.45(1+2+3)} + \underline{0.4 + 0.35*(4)} = 4.4$ ns

Max Delay $T_{CQ} + T_C + T_{setup} = 2 + 4.5 + 1 = 7.5$ ns

Delay due to temp.

$T_J = 25 + 1.5 * 30 = 70^{\circ}C$

$K_T = \left(\frac{70+273}{25+273}\right)^{1.5} = 1.23$

Max delay $T_{max} = 7.5 * 1.23$ ns $= 9.22$ ns

frequency $= \frac{1}{9.22} = 108.4$ MHz

c) Max frequency with −2 clock skew, Path D2-U1-D3 becomes the critical Path since only D3 has a skew w.r.t D2

$T_{max} = 5.5 + 2 + 1 = 8.5$

$8.5 * 1.23 = 10.455$ ns

$f_{max} = \frac{1000}{10.455}$ MHz $= 95.7$ MHz

Q6

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a) See notes

Start by use ieee. std_logic_1164.all

- define entity adder
- define 2 components Half Adder & OL gate
- define all signal within the architecture
- Port map components

- define entity test stimulator
- at behavior level using process

- Define test bench
- Components within test bench
- Port map components

b)