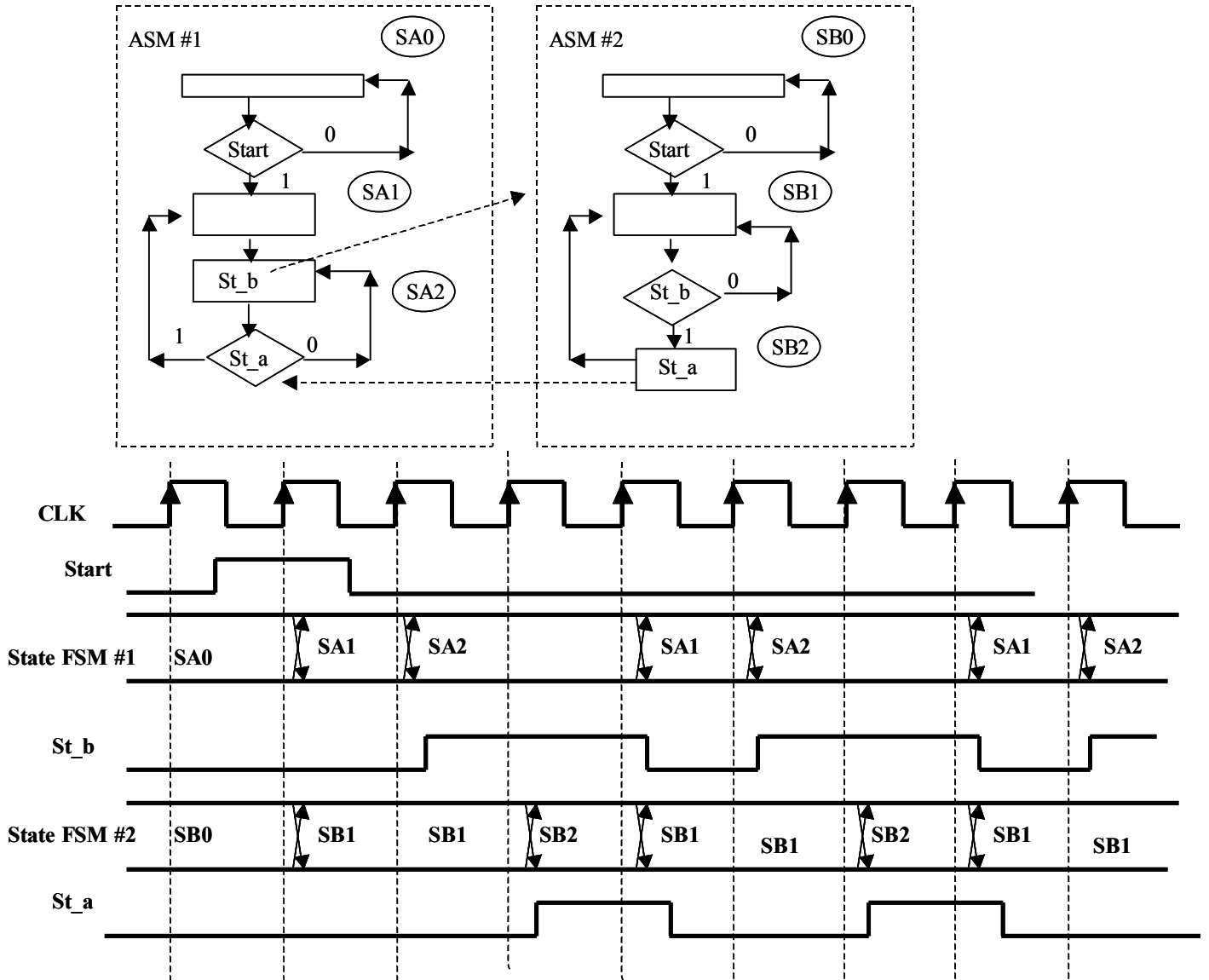


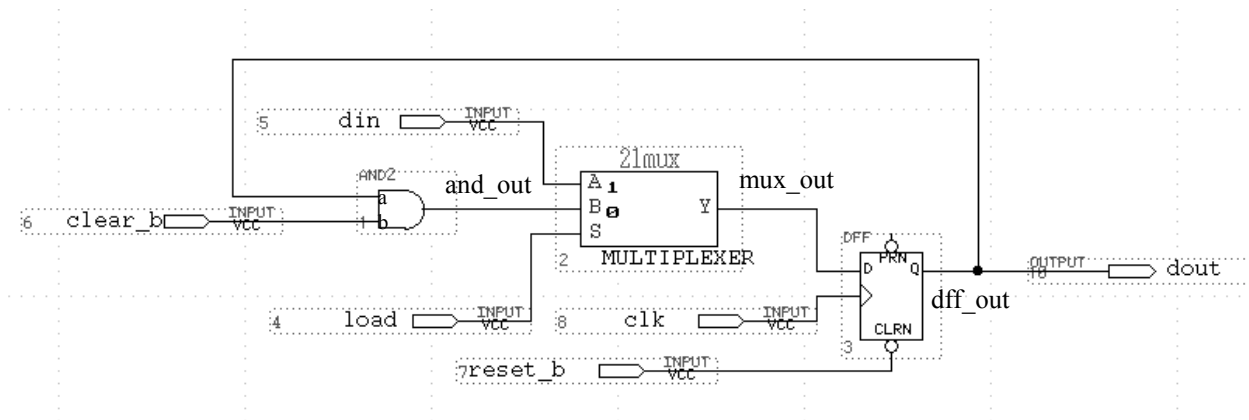
Student ID : \_\_\_\_\_ (no names please)

For any partial credit, you must show your work.

- (20 pts) Fill out all clock cycles for the timing diagram shown below for the cooperating finite state machines shown below:



2. (15 pts) Complete the structural VHDL model below to reflect the connections, instances in the schematic. The components declarations for the components are already given (I used a different name for the 2:1 mux because '2:1mux' is an illegal name in VHDL).



```
library IEEE;
use IEEE.std_logic_1164.all;
```

```
entity test is
  port ( din, clear_b, load, reset_b, clk: in std_logic;
        dout: out std_logic
        );
end test;
```

```
architecture a of test is
  component dff is
    port ( d,prn, clrn, clk: in std_logic;
          q: out std_logic );
  end component;
```

```
  component and2 is
    port ( a,b: in std_logic;
          y : out std_logic );
  end component;
```

```
  component mux2to1 is
    port ( a,b,s: in std_logic;
          y : out std_logic );
  end component;
```

```
  signal mux_out, dff_out, and_out: std_logic;
begin
  u1: and2
    port map (a=>dff_out, b=>clear_b, y=>and_out);

  u2: mux2to1
    port map (a=>din, b=>and_out, s=>load, y=>mux_out);

  u3: dff
    port map (d=> mux_out, clk=>clk, clrn=>reset_b,
             prn => open, q => dff_out);

  dout <= dff_out;
end a;
```

3. (20 pts) In class, we discussed the Xilinx PRO FGPA. This FPGA had a capability dubbed 'RocketIO' that supported some high-speed serial IO standards. Answer the following questions about the capabilities of this IO standard:

- a. Were the serial I/O standards differential, voltage referenced, or single-ended/full-rail standards?

differential

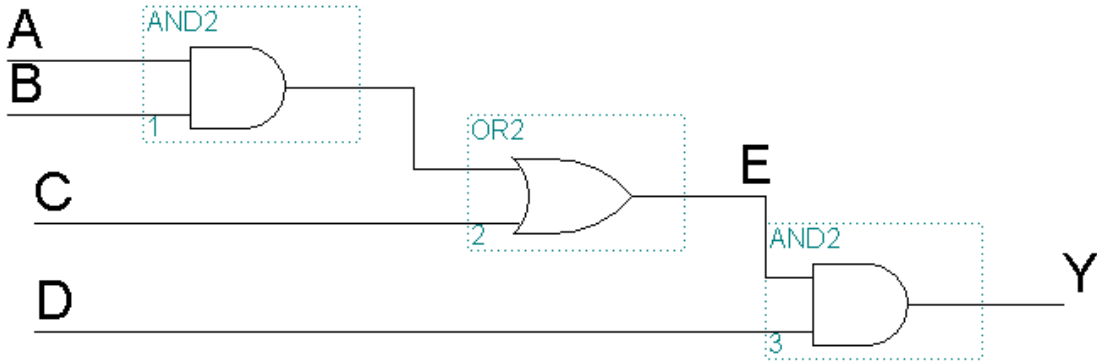
- b. DISCUSS how this serial I/O standards supported by the Rocket I/O logic guaranteed a particular transition density (1 to 0, or 0 to 1 transitions per unit time) in order to keep receiver circuitry synchronized? A one-or-two word answer is NOT sufficient -- this is a discussion question.

*The serial standards used 8B/10B coding which used 10 bits to encode 256 data values (D-characters) plus a few extra symbols (K-characters) for control flow. The extra 2 bits provides 1024 code combinations, and the code combinations were chosen so that no more than 5 consecutive '1's or '0's are possible regardless of the combination of characters.*

- c. The terms *DC-Balance*, and *disparity* are used to describe features of the supported serial I/O standards. What do these terms mean?

*disparity is the total number of '1's or '0's received over a some time period (a disparity of +1 would indicate that the number of '1's received was one greater then the number of zeros). DC-balance indicates that the number of '1's and '0's received of that period of time is the same.*

4. (5 pts) Give a test vector for the circuit below that will detect a STUCK-AT-1 fault on net E.



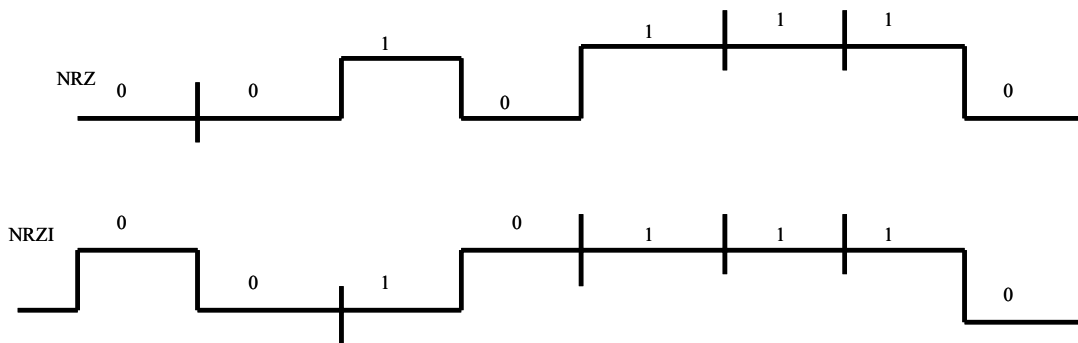
A=0, B=0, C=0, D=1. D = 1 so that node 'E' can be observed. C = 0', so that node E can be controlled by either A, or B. Setting both A and B to '0's means that the output Y should be a '0'; but it will be a '1' because of the stuck-at-1 fault at node E. A,B do not both have to be '0'; one of them as '0' is sufficient.

Answer 8 out of the following 11 questions. Circle/Cross out the questions that you DO NOT WANT GRADED.

5. What is the equivalent statement in Verilog for a VHDL *process* statement?

*an 'always' block*

6. Show how the bit stream (LSB) 00101110 (MSB) would be encoded in NRZI encoding. Assume the initial value of the serial output is a LOW Voltage. The bits are sent starting with the first bit on the LEFT and ending with the RIGHTMOST bit.



7. How does a scan path improve the controllability of a circuit?

*It allows the setting of the individual DFFs in the system (even if their inputs are buried) since all DFFs are connected into a shift register configuration (the scan path). The DFF values are set by asserting test mode = 1 and shifting in the new test vector.*

8. How does a scan path improve the observability of a circuit – be SPECIFIC.

*When the new test vector is shifted in the, result from the previous test stored in all of the DFFs are shifted out – we ‘observe’ the internal states of these DFFs which contain the results of the previous test vector.*

9. If a BIST scheme is used, give two different options for supplying test vectors to the device under test.

*Generating the test vectors via a linear-feedback-shift-register (LFSR), or reading the test vectors from an internal ROM.*

10. How do you compute the number of dots per line for a raster scan display given the dot clock frequency, the horizontal sync frequency, and the vertical sync frequency?

*number of dots = dot clock freq/ horizontal sync freq.*

11. What is a GENERIC MAP used for in a component instantiation in a structural VHDL model?

*It is used to pass parameter values to the VHDL model (ie, WIDTH => 8).*

12. What is an eye diagram used for in the testing of a serial transmission line?

*It is used to measure the quality of the serial transmission channel – an open eye indicates that the extracted clock signal frequency matches the received data transition frequency -- a closed eye means that the extracted clock edge is shifting due to line noise or clock jitter.*

13. What was a unique feature of the Cypress Microsystems PSOC that made it useful for a wide variety of single-chip applications that neither the the Xilinx Pro FPGA or any Altera FPGAs could address as a single chip solution?

*It contained programmable analog elements that could be used to implement D/A, A/D, comparators, etc.*

14. I classified the Cypress Microsystems PSOC as intended for low-end applications, and the Xilinx Pro FPGA as intended for high-end applications – why are these classifications appropriate?

*The Cypress PSOC only had an 8-bit CPU that ran at 24 MHz while the Xilinx PRO had a 32-bit CPU that ran at 300 Mhz.*

15. What does the JTAG 1149.1 standard concern?

*Defined a standard test port that could be used for boundary scan of ASICs on a printed circuit board.*