



## 8B/10B Coding (cont)

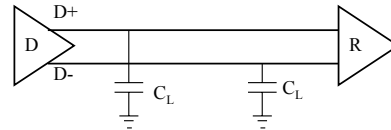
- Code is run length limited (RLL) – guarantees no more than five consecutive ‘1’s or five consecutive ‘0’s
  - Guaranteed transition density (transitions per unit time).
  - Allows receiver clock PLL to remain synchronized to input data stream
- *Disparity* – difference in number of received ‘1’s and ‘0’s in a serial stream over some length.
  - +1 disparity (one more ‘1’ than ‘0’)
  - -1 disparity (one more ‘0’ than ‘1’)
- Code is *DC-balanced* if equal numbers of ‘1’s and ‘0’s is sent.

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## LVDS

- LVDS – low voltage, differential signaling
  - Two lines: D+, D-
  - Signal swing is 300 mv, typically about 1.25V



For long lines, CL can be significant. If lines are quiescent (unchanging, high disparity) for a long period of time, charge builds up on CL. The energy in a single bit transition may not be enough to overcome this stored charge.

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## Disparity/DC-balance, and LVDS

- If a code has low disparity (low difference in number of ‘0’s, ‘1’s sent) then charge does not get chance to build up.
- For a given period of time, if equal numbers of ‘1’s, ‘0’s is sent, this is 0 disparity. This transmission is said to be ‘DC-balanced’.
- Each 10-bit symbols in the 8B/10B code either has a disparity of 0, +2 (six ones, four zeros), or -2 (four ones, six zeros)
- *Running Disparity* is the disparity for a given sequence of symbols, e.g. a packet
  - Disparity for a in a 10G ethernet packet is guaranteed to be either +1 or -1.

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## Error Detection

- CRC (Cyclic Redundancy Check) – much more complicated than a XOR checksum, much more robust in detecting errors
  - 32-bit CRC supported in RocketIO logic
- Running disparity can also be used to detect an error.

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## RocketIO Physical Interface

Table 4-1: Differential Transmitter Parameters

Parameter	Min	Typ	Max	Units	Conditions
V <sub>OUT</sub>	800		1600	mV	Output differential voltage is programmable
V <sub>VTX</sub>	1.8		2.8	V	
V <sub>FCM</sub>	1.5		2.5	V	
V <sub>SKENV</sub>			15	ps	

This is not LVDS standard as minimum differential is 800 mV.

Note large common-mode range.

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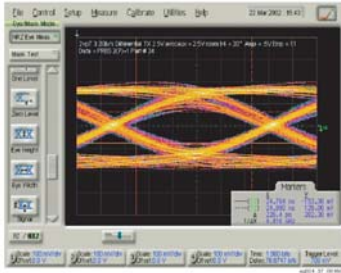
## Eye Diagram

- An EYE diagram used to measure quality of transmission channel.
- Generate pseudo-random data over channel, feed received data into vertical channel of scope
- Feed data rate (received generated clock) into horizontal sweep.
- An ‘open’ eye corresponds to minimal distortion.
- A closed eye shows signal *jitter*.
  - *Jitter* is short term variations of a signal from its ideal position in time.
  - Jitter caused by intersymbol interference, power supply noise, transmission channel loss, etc.

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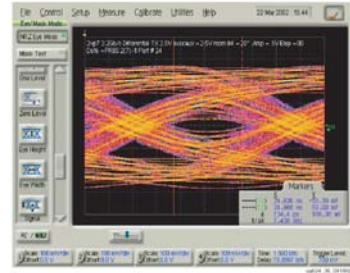
## Open Eye



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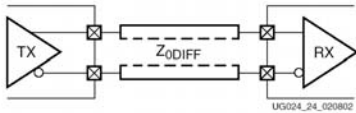
## Closed Eye



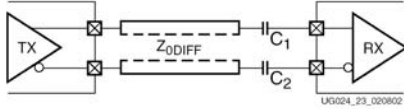
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## Connecting High Speed Serial Links



DC coupling – possible if same common voltages used.



Used if incompatible common-mode voltages or optical link is used. For AC coupling, *DC-balance* is very important because can't transmit signal with DC-content.

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## PowerPC 405-D Core

- Thirty-two 32-bit registers
- Load/Store instruction set
  - Multiply accumulate
  - Three timers
  - 64-bit time base for timers
- 16KB Icache, 16KB Dcache
- 5-stage pipeline (average of about 1 clock per instruction)
- Memory Management Unit (MMU) so can execute virtual memory Operating System (OS).
- No hardware floating point
- Operation at 300+ Mhz

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## PowerPC 405 Block Diagram

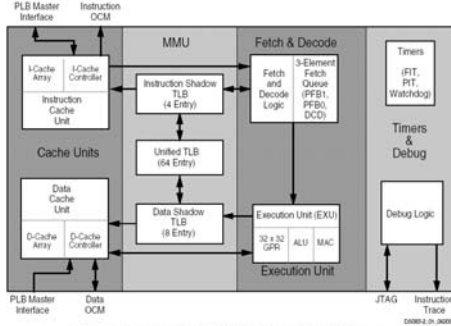


Figure 7: Embedded PPC405 Core Block Diagram

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## PowerPC core to FPGA connection

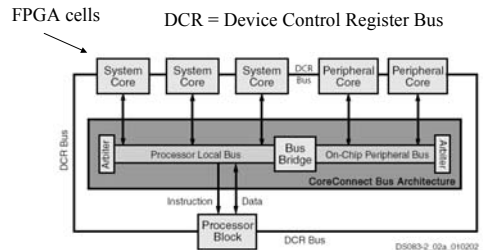


Figure 6: CoreConnect Block Diagram

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## Programmable System-on-a-Chip

- The Xilinx-II Pro and Cypress PSOC are two examples are programmable system-on-a-chip
- Processor core + programmable Logic is a powerful combination.
- Xilinx device intended for high-end, high-performance applications
- Cypress device for low-end, low-cost.