The Physical Reality

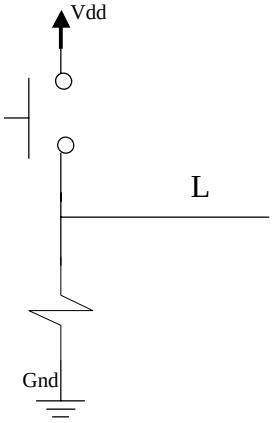
- So far, we have been viewing logic gates as paper/pencil abstractions
  - Does not do us much good in the real world.
- We need some method of physically implementing logic gates, and some way of representing digital quanties (1, 0) to these gates.
- There are many issues in the physical implementations of these logic functions
  - We can only look at a few of these issues, will try to cover the most important ones.

Representing ‘1’ and ‘0’

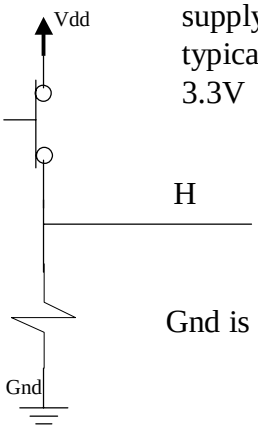
- In the electrical world, two ways of representing ‘0’ and ‘1’ are (these are not the only ways):
  - Presence or absence of electrical current
  - Different Voltage levels
- Different voltage levels are the most common
  - Usually 0v for logic ‘0’, some non-zero voltage for logic ‘1’ (I.e. > 3 volts)
- Can interface external sources to digital systems in many ways
  - Switches, buttons, other human controlled input devices
  - Transducers (change a physical quantity like temperature into a digital quantity).

Switch Inputs

High True switch



Switch open (**negated**), output is L

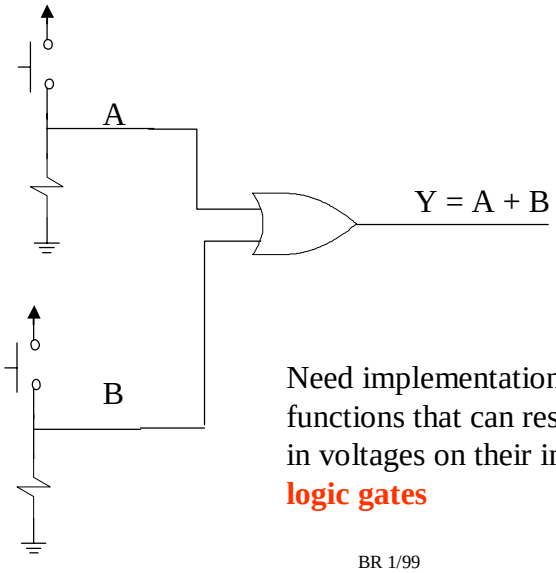


Vdd is power supply voltage, typically 5V or 3.3V

Gnd is 0 V

Switch closed (**asserted**), output is H

Voltage Logic Gates



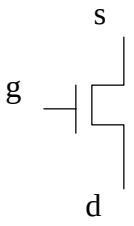
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	H

Need implementations of logic functions that can respond to changes in voltages on their inputs - **voltage logic gates**

What is inside of a voltage logic gate?

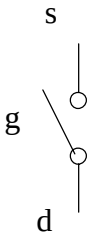
- Logic gates are made from transistors
  - TTL (Transistor-Transistor Logic) gates are made from Bipolar transistors
  - CMOS (Complementary Metal Oxide Semiconductor) logic gates are made from CMOS transistors
- One difference between CMOS and TTL gates is what voltage a 'H' is. For a power supply of 5V :
  - TTL: Minimum voltage for a 'H' is 2.4 V and input sinks (draws) current
  - CMOS: Minimum voltage for a 'H' is 3.2 V, input does not sink current.
  - Bipolar, CMOS transistors covered in Electronics I
  - Will get a brief introduction to CMOS transistors in this class.

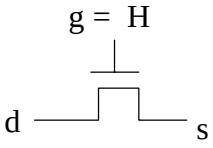
CMOS Transistors (N-type)

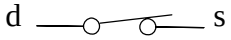


N-type (NMOS) transistor - can think of it as a switch.

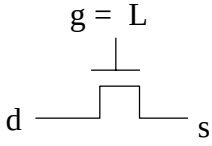
g: gate, d: drain, s: source

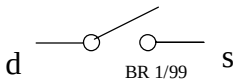






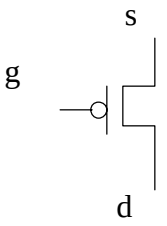
When g= H, d is connected to s (current flows between s, d because switch is closed.





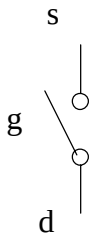
When g= L, d is disconnected from s (current does not flow between s, d because switch is open.

CMOS Transistors (P-type)

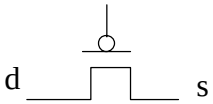


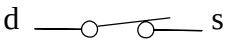
P-type (PMOS) transistor - can think of it as a switch.

g: gate, d: drain, s: source



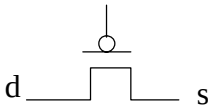
g = L

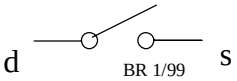




When g= L, d is connected to s (current flows between s, d because switch is closed.

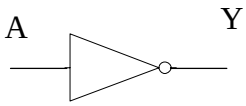
g = H

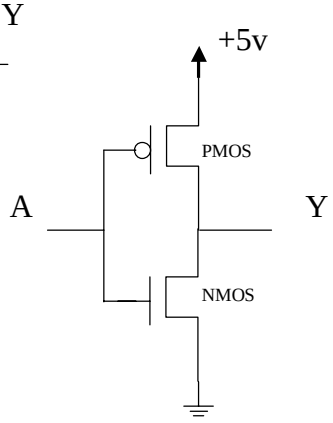




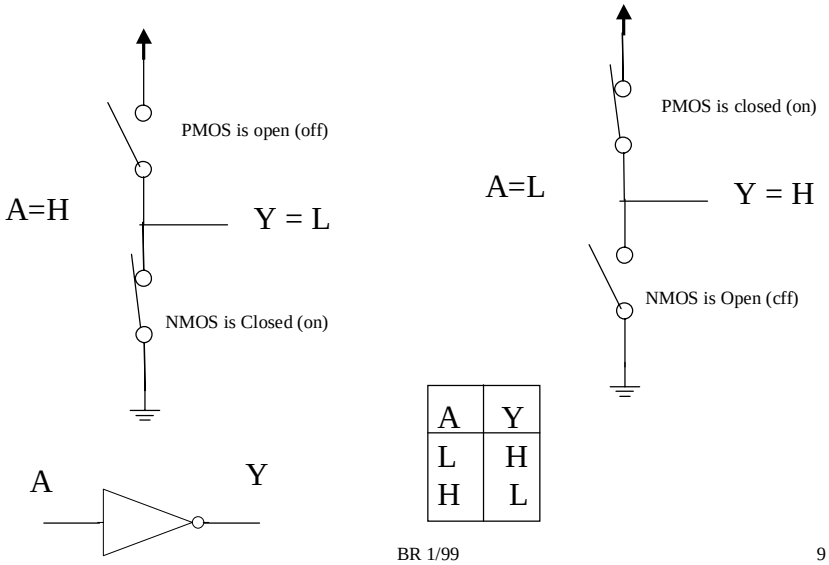
When g= H, d is disconnected from s (current does not flow between s, d because switch is open.

Inverter gate - takes 2 Transistors



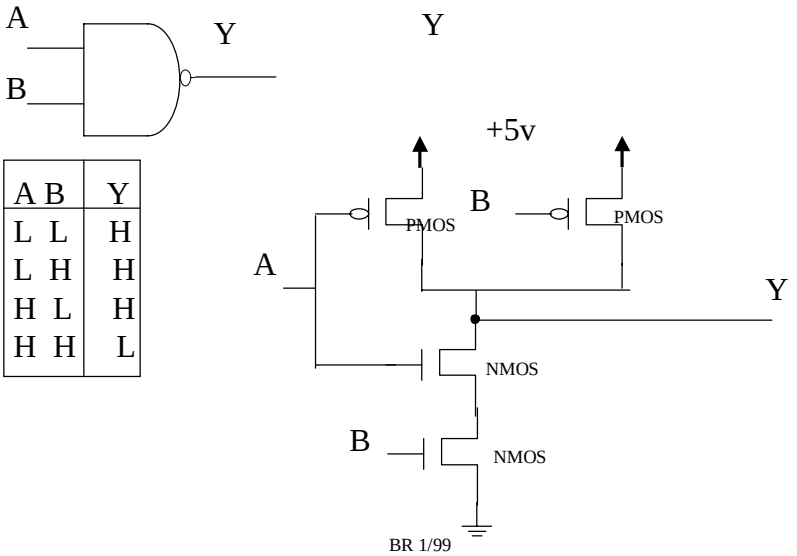


Inverter Operation



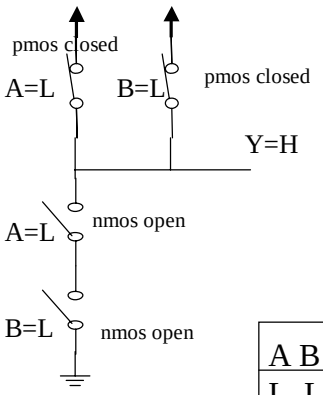
A	Y
L	H
H	L

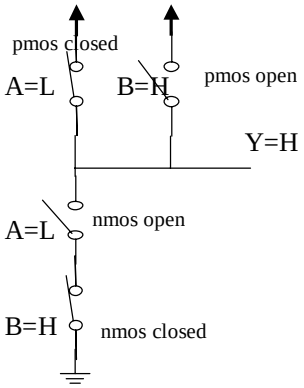
NAND gate - takes 4 Transistors



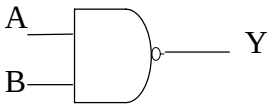
A B	Y
L L	H
L H	H
H L	H
H H	L

NAND Gate operation

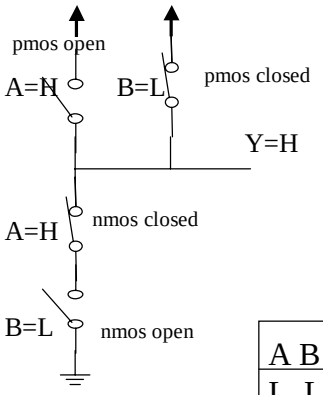


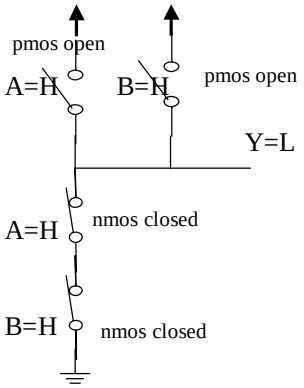


A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

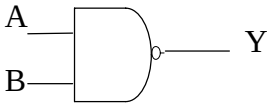


NAND Gate operation (continued)



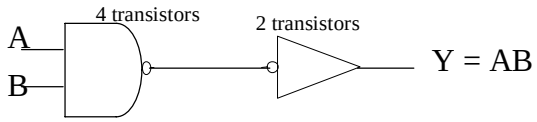


A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

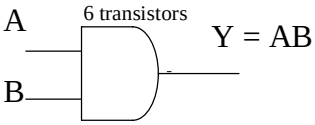


How do we make an AND gate?

The only way with CMOS transistors is to connect an inverter after a NAND gate.

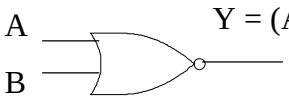


A B	Y
L L	L
L H	L
H L	L
H H	H

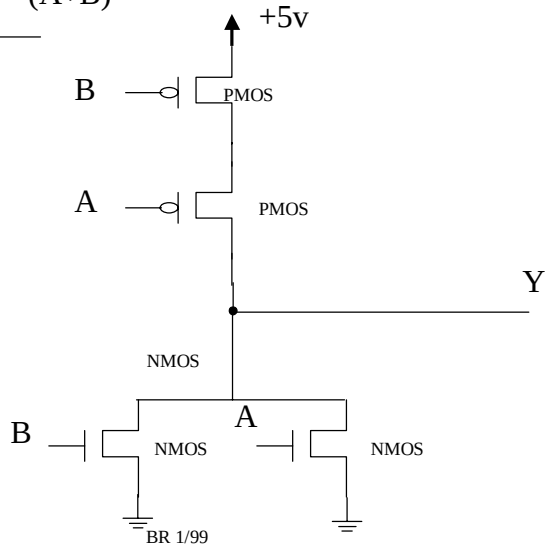


Takes 6 transistors! In CMOS technology, NAND gates are preferable to AND gates because they take less transistors, are faster, and consume less power.

NOR gate - takes 4 Transistors

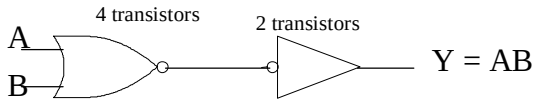


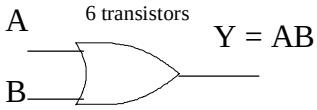
A B	Y
L L	H
L H	L
H L	L
H H	L



How do we make an OR gate?

The only way with CMOS transistors is to connect an inverter after a NAND gate.





A	B	Y
L	L	L
L	H	H
H	L	H
H	H	H

Takes 6 transistors! In CMOS technology, NOR gates are preferable to OR gates because they take less transistors, are faster, and consume less power.

Transistor Counts (CMOS)

Inverter:	2 transistors
Two input NAND:	4 transistors
Two input AND:	6 transistors
Two input NOR:	4 transistors
Two input OR:	6 transistors
Three input NAND:	6 transistors
Three input AND:	8 transistors
Three input NOR:	6 transistors
Three input OR:	8 transistors

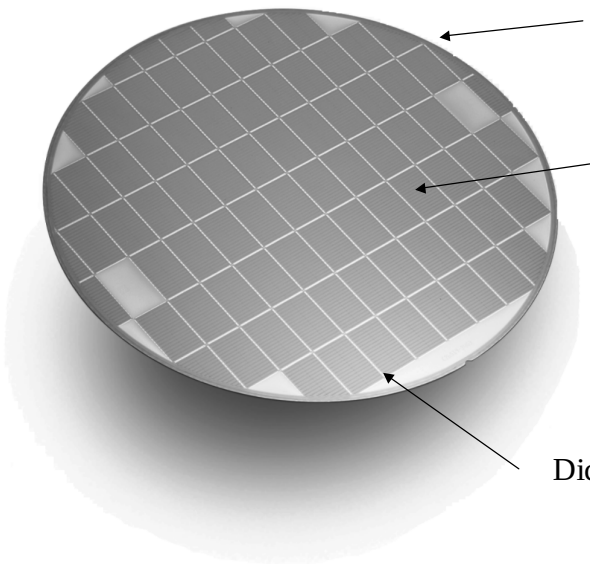
NAND, NOR gates are better than AND, OR gates because they take less transistors.

NAND gates better than NOR gates because they are faster (we won't discuss why, you will find out in Electronics I).

How are transistors fabricated?

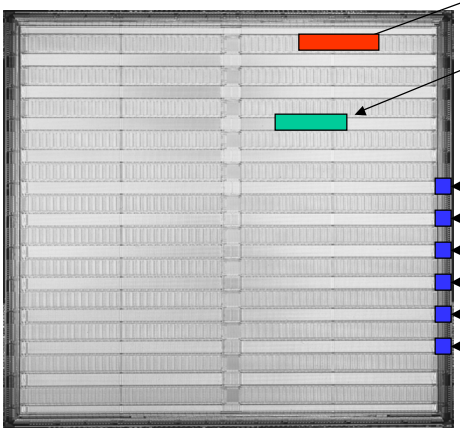
- Transistors and interconnections between transistors can be created via depositions of different materials onto a silicon wafer
  - Wafers are 6”, 8” in diameter depending on fabrication line
- Each wafer is divided into rectangular areas; each rectangle is called a **DIE** (plural is DICE).
  - Number of dice on a wafer depends on size of a die; anywhere from a few hundred to a few thousand dice on a wafer
- Each die can contain between a few thousand to a several million transistors (depends on size of the die).

Silicon Wafer



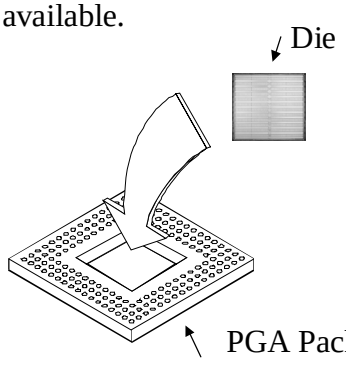
One Chip (a DIE)

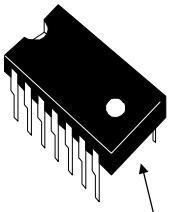
Die size can be anywhere from several centimeters (cm.) on a side to only a few tenths of a cm.



Packages

A die is placed in a package, the package provides connections to the external world. The 'die' is actually encased in the package; what is seen, handled by a person is actually the package. Many different package types are available.

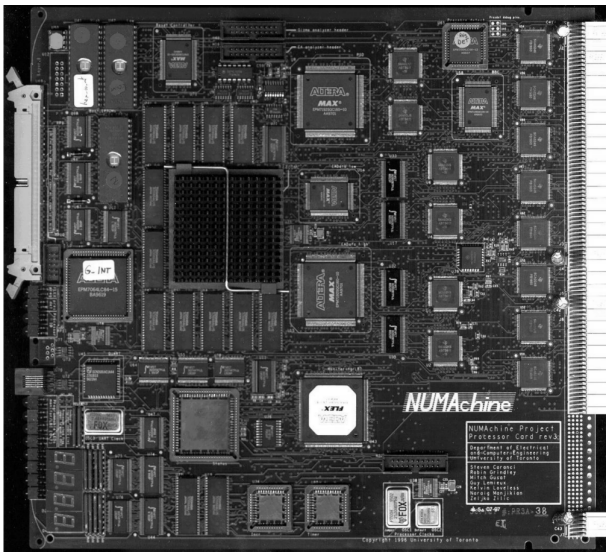




DIP Package
(Dual Inline Pins)

PGA Package (Pin Grid Array)

Printed Circuit Boards (PCBs)



Individual packages are then placed on a PCB; metal traces on and within the PCB provides interconnections between the packages.

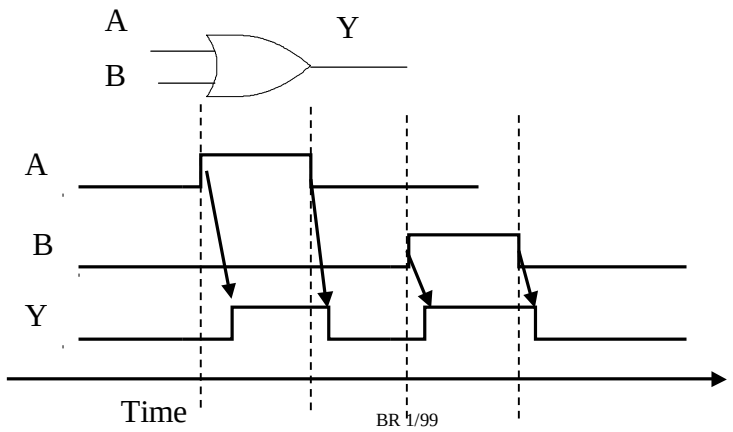
Other Physical Quantities

- Delay (speed). Transistors take a finite amount of time to switch. This means that a change on the input of a gate takes a finite amount of time to cause a change on the output.
- This time is known as **Propagation Delay**
- Smaller transistors means faster switching times. Semiconductor companies are continually finding new ways to make transistors smaller, which means transistors are faster, and more can fit on a die in the same area.

Timing Diagram

A timing diagram shows the signal state in a circuit over time.

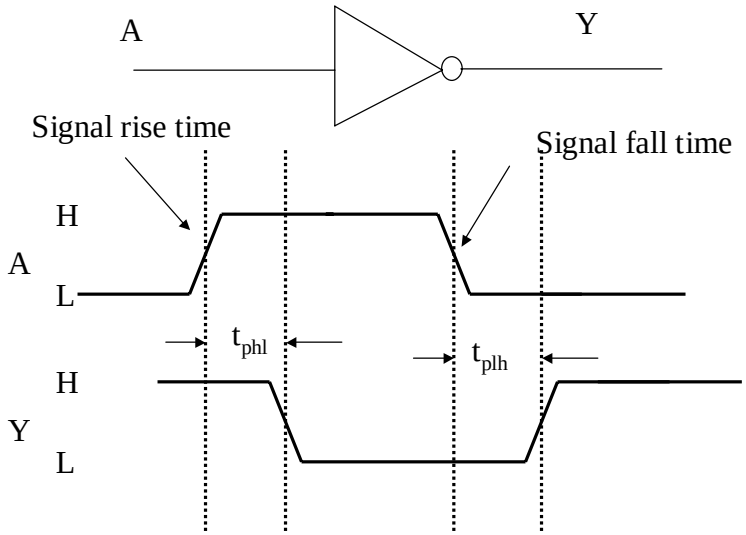
The vertical axis will be value (1 or 0), the horizontal axis is time.



Comments on Timing Diagram

- Will often use arrows from an input waveform to an output waveform to show what part of input waveform triggers a change on the output waveform
- Time axis will often have no units, just want to show functionality of logic
- Delay from an input change to an output change is **Propagation Delay**. Often a timing diagram will show a **zero** propagation delays even though actual prop delays will exist in the circuit.
- Signal edges are usually drawn vertically even though real signals have sloped edges (rise, fall times)

Propagation Delay (inverting)



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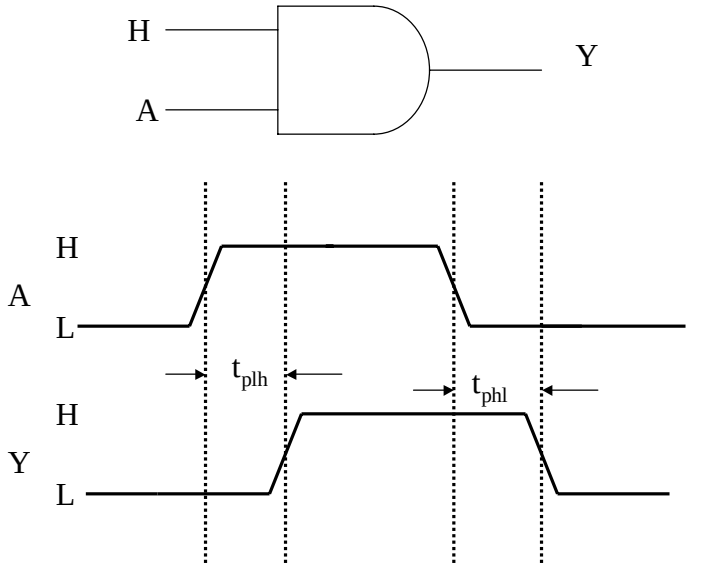
Propagation Delay (non inverting)



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Propagation Delay Definitions

- Tplh -- time between a change in an input and a low to high change on the output. Measured from 50% point on input signal to 50% point on the output signal. The 'lh' part (low to high) refers to OUTPUT change, NOT input change
- Tphl -- time between a change in an input and a high to low change on the output. Measured from 50% point on input signal to 50% point on the output signal. The 'hl' part (high to low) refers to OUTPUT change, NOT input change

In this Class….

- Will usually assume that Tplh = Tphl, and that all gates have same propagation delay
- Be aware that in real gates, this is NOT THE CASE.
- You will be expected to be able to draw a timing diagram for a combinational network of gates.

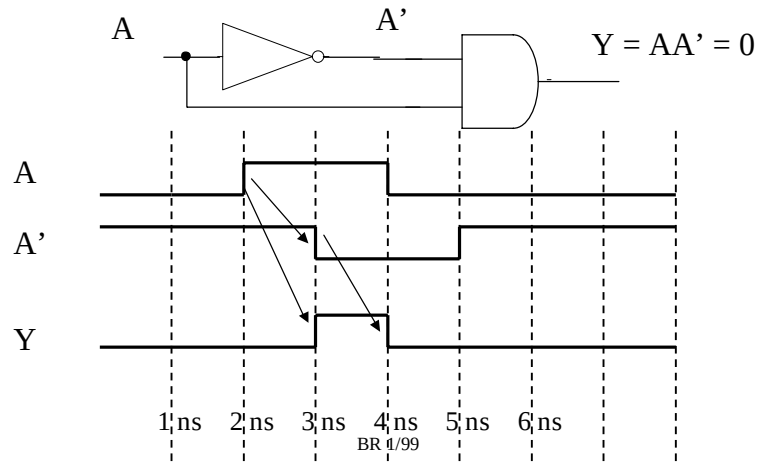
Time Units

1 s = 1 sec
1 ms = 1 millisecond = .001 sec = 1×10^{-3} s
1 us = 1 microsecond = .000001 sec = 1×10^{-6} s
1 ns = 1 nansecond = .000000001 sec = 1×10^{-9} s
1 ps = 1 picosecond = .000000000001 sec = 1×10^{-12} s

The gate delays for gates used in lab are a few nanoseconds. Gate delays on state-of-the-art high density logic devices are in the 10's to low hundreds of picoseconds.

Timing Diagram for a Network

Gate delays can cause unexpected results. In the circuit below, the output should always be ZERO, no matter what 'A' is. Assume each gate has a delay of 1 ns (1 nanosecond)

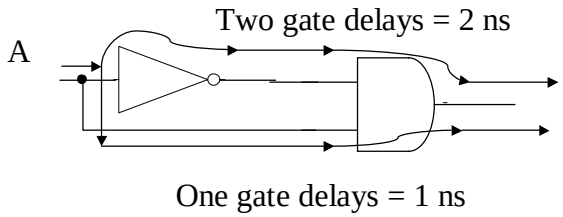


A Glitch!!

- Because the change in A was seen immediately at one input of the AND gate, but was delayed by the inverter on the other input, a **GLITCH** was caused at the output
- Glitches are caused by unequal path delays in a circuit
- Glitches are usually unavoidable, simply have to wait for 'settling time' before using output of circuit
  - Settling time is usually the worst case delay path

Delay Path

Simply add up the gate delays along each circuit path to get the worst case delay path of a circuit.



Worst case path delay is 2 ns.

Wires have delay also, but these are usually very short when compared to gate delays. We will ignore wire delays in this class.

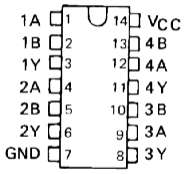
Datasheets and Databooks

A Datasheet provides pinout, functionality, and operating characteristics (timing, power, voltage specs, etc) for the device.

A Databook is simply a collection of datasheets for a particular product family.

7400 Data Sheet -- Pinout, Functionality

SN7400 . . . N PACKAGE
SN74LS00, SN74S00 . . . D OR N PACKAGE
(TOP VIEW)



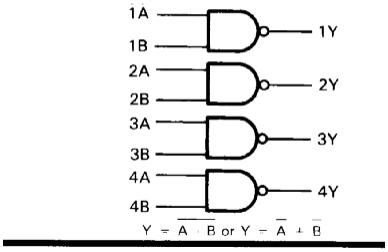
SN5400 . . . W PACKAGE
(TOP VIEW)

FUNCTION TABLE (each gate)

INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

NC - No internal connection

logic diagram (positive logic)



7400 contains 4 NAND gates. One package available is a 14 pin DIP. A 7400 is a TTL Device.

Maximum Ratings

Maximum ratings are absolute Vdd, Input voltage ratings for device without DAMAGE. These are not recommended operating conditions.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage: '00, 'S00 . . . . . 5.5 V
'LS00 . . . . . 7 V
Operating free-air temperature range: SN54' . . . . . −55°C to 125°C
SN74' . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

Recommended Operating Conditions

The input, Vdd voltages for which the timing, power specs are valid for.

recommended operating conditions

		SN5400			SN7400			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−0.4			−0.4	mA
I_{OL}	Low-level output current			16			16	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

V_{IH} - minimum input voltage that will be recognized as a 'H'.

V_{IL} - maximum input voltage that will be recognized as a 'L'.

Electrical Characteristics

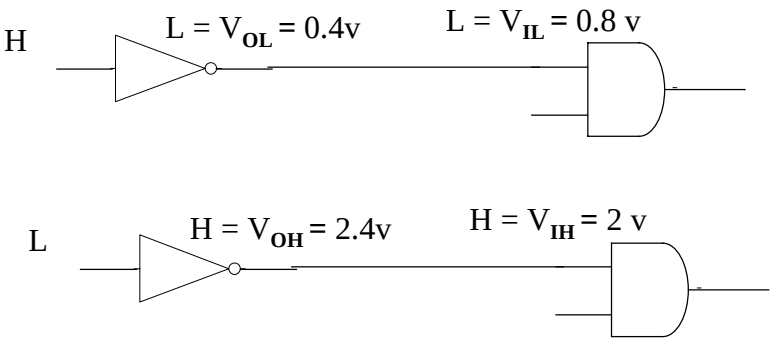
electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN5400			SN7400			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = MIN, I_I = – 12 mA			– 1.5			– 1.5	V
V_{OH}	V_{CC} = MIN, V_{IL} = 0.8 V, I_{OH} = – 0.4 mA	2.4	3.4		2.4	3.4		V
V_{OL}	V_{CC} = MIN, V_{IH} = 2 V, I_{OL} = 16 mA		0.2	0.4		0.2	0.4	V
I_I	V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	V_{CC} = MAX, V_I = 2.4 V			40			40	μA
I_{IL}	V_{CC} = MAX, V_I = 0.4 V			– 1.6			– 1.6	mA
I_{OS}§	V_{CC} = MAX	– 20		– 55	– 18		– 55	mA
I_{CCH}	V_{CC} = MAX, V_I = 0 V		4	8		4	8	mA
I_{CCL}	V_{CC} = MAX, V_I = 4.5 V		12	22		12	22	mA

V_{OH} : minimum output Voltage for a 'H'
V_{OL}: maximum output Voltage for a 'L'
I_{IH} : Input high current, I_{IL} : Input Low current

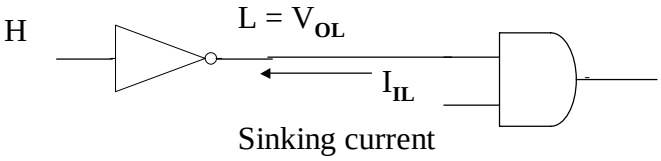
Negative I_{IL} means that we are drawing current from input.

V_{OH}, V_{OL} versus V_{IH}, V_{IL}

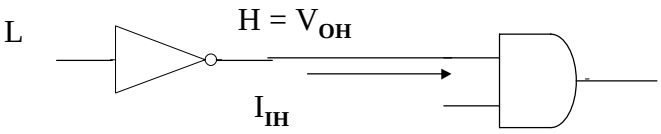


Note that $V_{OL} < V_{IL}$, $V_{OH} > V_{IH}$. This is for noise immunity purposes.
$V_{IL} - V_{OL}$ is the Low Noise Margin.
$V_{OH} - V_{IH}$ is the High Noise Margin.

Electrical Characteristics



Sinking current



Sourcing current

Propagation Delay

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	A or B	Y	R_L = 400 Ω, C_L = 15 pF		11	22	ns
t_{PHL}					7	15	ns

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

Both Vdd and Temperature will affect propagation delay.

Higher Vdd, faster switching (can't go too high, will damage device, excessive power consumption).

Lower Temp, faster switching.

CMOS 7400 Electrical Characteristics

PARAMETER	SYMBOL	TEST CONDITIONS V_I (V)	TEST CONDITIONS I_O (mA)	V_{CC} (V)	25°C MIN	25°C TYP	25°C MAX	-40°C TO 85°C MIN	-40°C TO 85°C MAX	-55°C TO 125°C MIN	-55°C TO 125°C MAX	UNITS
HC TYPES												
High Level Input Voltage	V_{IH}	-	-	2	1.5	-	-	1.5	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	3.15	-	V
				6	4.2	-	-	4.2	-	4.2	-	V
Low Level Input Voltage	V_{IL}	-	-	2	-	-	0.5	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	-	1.35	V
				6	-	-	1.8	-	1.8	-	1.8	V
High Level Output Voltage CMOS Loads	V_{OH}	V_{IH} or V_{IL}	-0.02	2	1.9	-	-	1.9	-	1.9	-	V
			-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
			-0.02	6	5.9	-	-	5.9	-	5.9	-	V
Low Level Output Voltage CMOS Loads	V_{OL}	V_{IH} or V_{IL}	-4	4.5	-	-	0.1	-	0.1	-	0.1	V
Input Leakage Current	I_I	V_{CC} and GND	4	5.5	-		±0.1	-	±1	-	±1	µA
Quiescent Device Current	I_{CC}	V_{CC} or GND	0	5.5	-	-	2	-	20	-	40	µA

Switching Characteristics

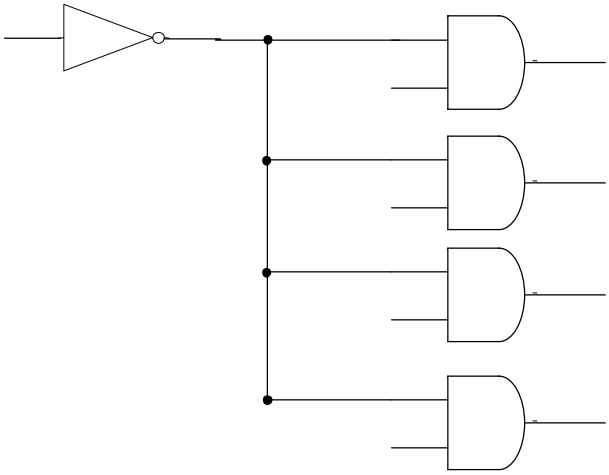
CD54HC00, CD54HCT00, CD74HC00, CD74HCT00

Switching Specifications Input t_r, t_f = 6ns **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	V_{CC} (V)	25°C MIN	25°C TYP	25°C MAX	-40°C TO 85°C MIN	-40°C TO 85°C MAX	-55°C TO 125°C MIN	-55°C TO 125°C MAX	UNITS
Transition Times (Figure 1)	t_{TLH}, t_{THL}	C_L = 50pF	2	-	-	75	-	95	18	110	ns
			4.5	-	-	15	-	19	-	22	ns
			6	-	-	13	-	16	-	19	ns
Input Capacitance	C_I	-	-	-	-	10	-	10	-	10	pF
Power Dissipation Capacitance (Notes 3, 4)	C_{PD}	-	5	-	25	-	-	-	-	-	pF
HCT TYPES											
Propagation Delay, Input to Output (Figure 2)	t_{PLH}, t_{PHL}	C_L = 50pF	4.5	-	-	20	-	25	-	30	ns
Propagation Delay, Data Input to Output Y	t_{PLH}, t_{PHL}	C_L = 15pF	5	-	8	-	-	-	-	-	pF
Transition Times (Figure 2)	t_{TLH}, t_{THL}	C_L = 50pF	4.5	-	-	15	-	19	-	22	ns
Input Capacitance	C_I	-	-	-	-	10	-	10	-	10	pF
Power Dissipation Capacitance (Notes 3, 4)	C_{PD}	-	5	-	25	-	-	-	-	-	pF

Fanout

Fanout is the number of gate inputs an output is driving



Fanout Limits

There is a limit to the number of gate inputs a single output can drive.

For TTL, the limit is based on CURRENT. A TTL output can supply I_{OL} = 16 ma (milliamps) Maxium. A TTL input I_{IL} is -1.6ma. Maximum fanout for TTL is 16ma/1.6 ma = 10 loads.

For CMOS, the limit is based on SPEED. A CMOS input looks like a capactive load (10 pf - picofarads). The more INPUTs tied to a single OUTPUT, the higher the capactive load. The HIGHER the capacitive load, the slower the propagation delay. Typically, try to avoid loads much higher than about 8 loads.

Other CMOS/TTL Differences, Facts

CMOS gates can run at a wide range of voltages. Note that the CMOS datasheet had specs for Vcc = 2V, 4.5 V, 6 V.

TTL gates tolerate only a narrow Vdd range (4.5 to 5.5v).

TTL gates (bipolar transistors) will generally switch faster than CMOS gates (but TTL gates consume too much power at high gate counts).

When TTL gates are quiescent (inputs are not switching), they are still drawing current and consuming power.

When CMOS gates are quiescent (inputs are not switching), they are not drawing current (only a very small amount of leakage current). CMOS gates consume power only when switching; the faster the clock rate, the more power consumed. CMOS gates are preferable for low power applications.

Fanin Limitations

A physical gate cannot have a large number of inputs (fanin).

- The more inputs that a CMOS gate has, generally the slower the device
  - A 4-input NAND gate is slower than a 2-input NAND gate
- In CMOS technology, generally do not build greater than 4 input gates
  - More than 4 inputs makes the devices too slow because end up having too many transistors in series.
  - TTL gates can have more inputs (8 input NAND 7430)
- Have to design logic knowing the input limitations.

Some Common 74xx gates

- 7404 - inverter
- 7400 (2-input NAND), 7402 (2 Input Nor)
- 7408 (2-input AND), 7432 (2-input OR)
- 7410 (3-input NAND)
- 7486 (2-input XOR)
- 7420 (4 input NOR)

What do you have to know?

- CMOS, TTL Technology basics
- NAND, NOR, Inverter CMOS transistor diagrams
- Packages vs chips
- Propagation delay
- Timing diagrams
- How to read a datasheet (timing specs, electrical specs)
- CMOS, TTL Fanout limitations
- Fanin limitations