

Dice Game Implementation

- Dice game implemented in three 22V10 PLDs
 - control.vhd (Finite State Machine)
 - dpatha.vhd (two 1-6 counters, adder)
 - dpathb.vhd (point register, comparator, test logic)
- The Control FSM is implemented using one-hot encoding.
 - Outputs q0, q1, q5 are states S0, S1, S5. Output “win” is state S2, output “lose” is state S3. Outputs q0,q1,q5 are available just for debugging purposes.

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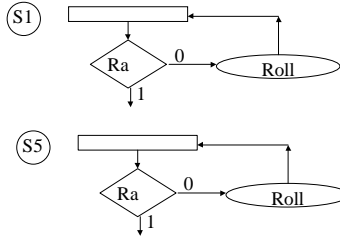
Finite State Machine Changes

Asynchronous Reset now use to exit states S2, S3. Resets back to State S0.

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Finite State Machine Changes (cont).

Because we don't have debounced switches, added extra "roll" input called "Ra". Changed States S1, S5 to use Ra, not Rb.



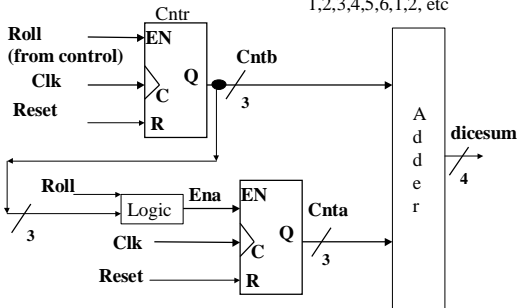
This means that to roll the dice, you use flip switch Rb up, then down. This starts the dice rolling. To stop the dice, Flip Ra switch up then down.

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"dpatha" Details

Counters count 1,2,3,4,5,6,1,2, etc

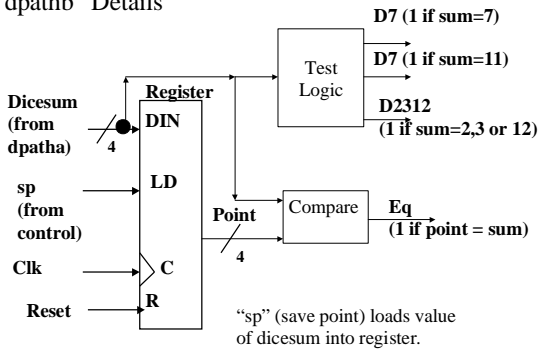


Ena = 1 when Cntb = 6 and Roll = 1

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"dpathb" Details



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