RASSP Benchmark-1 and -2: A Preliminary Assessment*

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Abstract

These two benchmarks required the development of a virtual prototype and a hardware prototype, respectively, of a Synthetic Aperture Radar processor. The two RASSP Developers chose different approaches: one used COTS components on custom boards with a methodology emphasis on detailed VHDL prototyping and board design and one used COTS computer boards with a methodology emphasis on efficient VHDL modeling and automatic code generation. Both efforts are briefly described. A preliminary assessment of Benchmark-1, which has been completed, is offered with emphasis on the experience with VHDL modeling. Based on this assessment, some recommendations for improvement are made.

1: Introduction

The benchmarking component of the RASSP program is designed to evaluate the process, tool integration, and products developed, and to report the results to the Developers, sponsors and other interested parties[1]. In the course of the RASSP program, several application threads will be selected and design exercises defined for up to six benchmarks. MIT Lincoln Laboratory developed the specifications for Benchmark -1 and -2, and is observing and measuring the Developers' performance. The first application thread is a Synthetic Aperture Array (SAR) signal processor. Benchmark-1 requires that the developers perform trade-offs of several architectures and create a VHDL virtual prototype of their selected design. Construction of a physical (hardware) prototype of the SAR processor is required in Benchmark-2. Benchmark-1 has been completed and Benchmark-2 is scheduled for completion in August, 1995. This paper reports some of the conclusions from Benchmark-1, some early observations of Benchmark-2, and comments on the benchmark process.

2: Benchmark Process

Lincoln Laboratory acts as the customer for the benchmarks. The deliverables include not only the virtual and hardware prototypes, but also extensive metric data on the design process, tool use and final products, as well as financial data. Besides participating in the periodic program reviews, Lincoln Laboratory personnel attend internal meetings, interview benchmark personnel, and collect copies of work in progress at defined milestones.

In addition to the usual documents prepared by a customer (a technical description, a list of deliverables and contractual details), Lincoln delivered a VHDL Executable Requirement at the beginning of Benchmark-1. During Benchmark-2, Lincoln will deliver to the Developers a hardware source/sink[1] with which to test the prototype.

3: SAR Processor

The processor specified for the SAR application thread is required to form images in real time on board an unmanned air vehicle, and to be compatible with the data rates and format of the Lincoln Laboratory Advanced Detection Technology Sensor (ADTS)[2]. The ADTS radar is a fully polarimetric air-to-ground SAR that operates in both "spotlight" and "stripmap" mode; only the stripmap mode is employed for RASSP. The processor can be partitioned into seven functional blocks:

1. Preamble detection and extraction of radar and auxiliary data from the input data stream.

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2. Video to baseband I/Q conversion.
3. Range processing.
4. Corner turn.
5. Azimuth processing.
6. Output data formatting.
7. Command processing, control and test.

At its maximum PRF of 556 Hz, the radar delivers 512 pulses with 4064 data samples for each of the four polarizations in 0.92 seconds. The processor must be able to form a 512-pulse image for each of *three* polarizations in real time with a latency not greater than three seconds. The processor can be set up to use anywhere from an 8 to a 48 tap FIR filter in it's video to baseband I/Q conversion. With a baseline algorithm the computational requirement with the 8 tap filter is about 1.1 Gflop/second, and with the 48 tap filter about 2.0 Gflop/second.

The processor must conform to a 10.5" × 20.5" × 17.5" space with expansion space for twice the computational throughput, weigh less than 60 pounds, use less than 500 watts on average, and be designed to operate on-board a small aircraft. Test requirements were "best practice".

4: Benchmark-1

The product of Benchmark-1 was described this way in the Benchmark-1 Technical Description[3]:

> Each RASSSP developer shall investigate at least two prototype processor designs, one minimizing cost to produce in prototype quantities, and the other minimizing processor power and weight. Both designs shall be developed to the point where realistic estimates of performance can be made. Use of VHDL performance modeling to substantiate the performance estimates is desired. Both designs must also be producible in unit quantities within the time and effort constraints established for Benchmark-2.
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> One of the architectural concepts investigated at the performance model level shall be selected by the Developer for evolution to a virtual prototype as described in 1.1.1. Insofar as possible, subject to the six month duration and 5000 hour equivalent level of effort established for Benchmark-1, the virtual prototype shall emulate the critical behavior and timing of the selected design.

The Section 1.1.1 referenced above defined virtual prototype in the following manner[3]:

> As used here, a virtual prototype is an executable software model of an embedded processor which represents all of the important function and timing information of the processor with sufficient fidelity to insure that the processor will perform as intended when constructed in accordance with the architecture underlying the virtual prototype model. … One of the principal issues of interest in Benchmark-1 is the degree of fidelity and completeness that can be obtained for reasonable cost using existing virtual prototyping methodologies and models. The expectation is that IEEE-compliant VHDL simulation will be the vehicle for developing the virtual prototype. The level of detail and fidelity attained in the virtual prototype will be limited by the constraints of time (6 months) and level of effort (5000 person-hours) imposed for Benchmark-1. One of the responsibilities which the Developers have under the RASSP program is to establish cost-effective methodologies and tools for the creation and application of virtual prototypes to the development of embedded signal processing systems.

4.1: Executable Requirement

At the beginning of Benchmark-1 Lincoln Laboratory delivered to the Developers an Executable Requirement (ER)[4][5]. It was a VHDL behavioral model of the processor which implemented one possible algorithm. The ER modeled timing at the input and output data ports, and throughput latency. A VHDL test bench sourced commands and data from disk files, compared data outputs with supplied image files, wrote outputs to disk files, and checked latency of the processor. Data files from the ADTS radar and a synthetic data set were supplied, as were reference image files which had been generated by a C-language simulation of the SAR processor. The C simulator was not distributed. An image-pixel based limit on the difference between the reference processor images and the generated images was specified with an option given for the Developers to define and validate any other reasonable error metric. (Both Developers accepted the limit definition.) T