ProASIC^{PLUS} Starter Kit

User's Guide & Tutorial

Actel

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Table of Contents

Introduction

Thank you for purchasing Actel's ProASIC^{PLUS} Starter Kit.

This guide provides the information required to easily evaluate the ProASIC^{PLUS} devices. This is the first release of the *Starter Kit User's Guide*. The most up-to-date version of this guide is available at:

http://www.actel.com/techdocs/manuals/default.asp

Document Contents

Chapter 1 - Contents and System Requirements describes the contents of the ProASIC^{PLUS} Starter Kit.

Chapter 2 - Hardware Components describes the components of the ProASIC^{PLUS} Evaluation Board.

Chapter 3 - Setup and Self Test describes how to setup the ProASIC^{PLUS} Evaluation Board and how to perform a self test.

Chapter 4- Actel VHDL APA Design Flow introduces the design flow for VHDL using the Actel Libero™ Integrated Design Environment (IDE) suite.

Chapter 5- Quick Start Tutorial contains a step-by-step tutorial.

Appendix A - Board Connections provides a table listing the board connections.

Appendix B - Board Schematics provides illustrations of the ProASIC^{PLUS} Evaluation Board.

Appendix C - Product Support describes Actel's support services.

Document Assumptions

This user's guide assumes:

- You intend to use Actel's Libero IDE software.
- You have installed and are familiar with Actel's Libero IDE 5.0 software.
- You are familiar with the VHDL hardware description language.
- You are familiar with PCs and Windows operating systems.

1

Contents and System Requirements

This chapter details the contents of the ProASIC^{PLUS} Starter Kit and lists the power supply and software system requirements.

Starter Kit Contents

The starter kit includes:

- Evaluation board - APA-EVAL-BRD075
- Libero IDE Gold
- FlashPro Lite
- The *ProASIC^{PLUS} Starter Kit User's Guide & Tutorial*
- Customer Letter
- CD with design examples
- Switching brick power supply, part number DTS090220U-P5P-SZ from CUI INC

For the CD contents, review the ReadMe.doc file at the top level of the CD.

2

Hardware Components

This chapter describes the hardware components of the ProASIC^{PLUS} Evaluation board.

ProASIC^{PLUS} Evaluation Board

Figure 2-1 illustrates a top-level view of the ProASIC^{PLUS} Evaluation board.

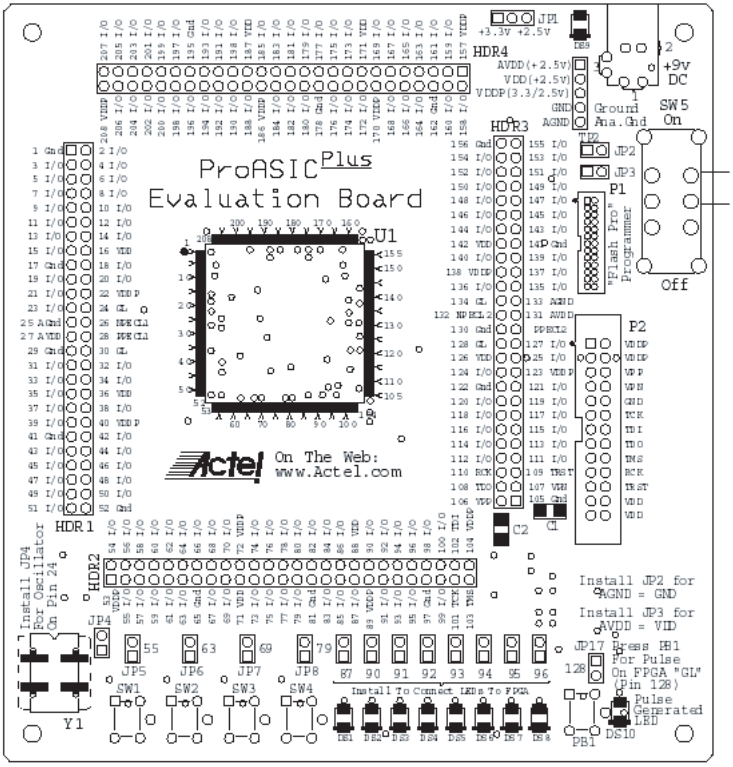


Figure 2-1. ProASIC^{PLUS} Evaluation Board: Top-Level View

The ProASIC^{PLUS} evaluation board consists of:

- Wall mount power supply connector, with switch and LED indicator
- Jumper to select between 2.5V and 3.3V I/O voltages
- Small program header (compatible with both FlashPro/FlashPro Lite and Silicon Sculptor)
- 40MHz oscillator and manual clock option
- Eight LEDs (driven by outputs from the device)
- Jumpers (allow disconnection of all external circuitry from the FPGA)
- Four switches (provide input to the device)

For further information, refer to the following appendices:

Appendix A – Board Connections

Appendix B – Board Schematics

Power Supply

To use the ProASIC^{PLUS} Evaluation board with a wall mount power supply, use the switching brick power supply that is provided with the kit. The power supply is controlled by an On/Off switch. An LED DS9 indicates the presence of a working wall mount supply.

- Use **JP1** to select either 3.3V or 2.5V for the Device I/O Voltage.
- **JP2** connects AGND to GND for the use of the PLL.
- **JP3** connects AVDD to VDD for the use of the PLL.

  Note: Alternatively, use the five pin header next to the power supply connection to drive power to the board from a laboratory supply.

Programming Headers

A small form programming header, which is suitable for use with both the FlashPro/FlashPro Lite and Silicon Sculptor II, is supplied with the board. The

footprint for the large programming header is on the board, but has not been populated.

When using FlashPro/FlashPro Lite, use the STAPL(.STP) file to program the device. Silicon Scluptor II can be used for both bitstream (.BIT) or STAPL (.STP) files. However, the ISP programming adapter module SMPA-ISP-ACTEL-3-KIT is required to use Silicon Sculptor II with the ProASIC^{PLUS} Evaluation board.

Clock Circuits

The ProASIC^{PLUS} Evaluation board has two clock circuits, a 40MHz oscillator and a manual clock.

40MHz Oscillator

The 40MHz oscillator on the board is connected to JP4. JP4 connects the clock to pin 24 of the devices. Pin 24 is a global input pin. To use pin 24 for a different clock signal, disconnect JP4.

To use a different Clock Frequency, purchase the Crystal from Epson programmed to a variety of frequencies. The SG-8002JC40.000M-PCC from Epson is also available through Digikey.

Manual Clock

When activated, the manual clock button (PB1) lights DS10, the pulse generated LED, and generates a pulse. This is connected to JP17. JP17 connects to pin 128 of the device. Pin 128 is a global input pin.

To use pin 128 for a different clock signal, disconnect JP17.

LED Device Connections

Eight LEDs are connected to the device via jumpers. If the jumpers are in place, the device I/O can drive the LEDs. The LEDs change based on the following output:

- A ‘1’ on the output of the device lights the LED.
- A ‘0’ on the output of the device switches off the LED.

- An unprogrammed or tristated output may show a faintly lit LED.

Table 2-1 lists the LED/device connections.

To use the device I/O for other purposes, remove the jumpers.

Table 2-1. LED Device Connections

LED	Device Connection
DS1	Pin 87
DS2	Pin 90
DS3	Pin 91
DS4	Pin 92
DS5	Pin 93
DS6	Pin 94
DS7	Pin 95
DS8	Pin 96

Figure 2-2 illustrates the location of the LED/device connections on the ProASIC^{PLUS} evaluation board.

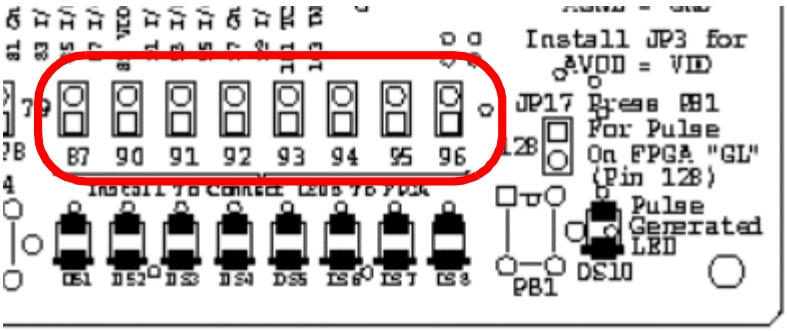


Figure 2-2. LED Device Connections

Switches Device Connections

Four switches are connected to the device via jumpers. If the jumpers are in place, the device I/O can be driven by the switches listed in Table 2-2.

- Pressing a switch drives a 1 into the device. The 1 continues to drive while the switch is in place.
- Releasing a switch drives a zero into the device.

Table 2-2 lists the switch/device connections.

To use the device I/O for other purposes, remove the jumpers.

Table 2-2. Switch Device Connections

Switch	Device Connections
SW1	Pin 55
SW2	Pin 63
SW3	Pin 69
SW4	Pin 79

Figure 2-3 illustrates the switch device connections.

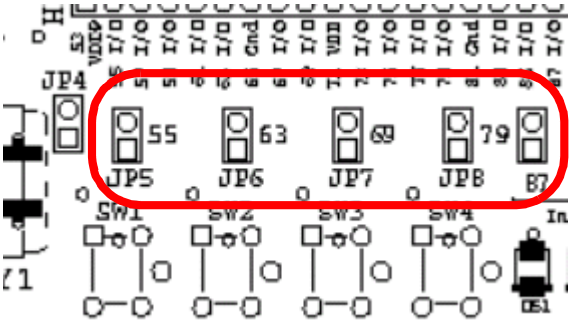


Figure 2-3. Switch Device Connections

3

Setup and Self Test

This chapter outlines how to set up and test the ProASIC^{PLUS} Evaluation Board.

Software Installation

The ProASIC^{PLUS} Starter Kit includes the Libero™ Integrated Design Environment (IDE) software (version 5.0). For Libero IDE software installation instructions and license, refer to the Actel Installation and Licensing Guide at:

http://www.actel.com/documents/install.pdf

This User's Guide uses VHDL language. Please select "Install/Modify VHDL"as shown in Figure 3-1 [1]

Note: The Libero Gold package includes Synplicity Synplify AE 7.3. In order to setup the license you need to use LM_LICENSE_FILE variable. Please see "Actel Installation and Licensing Guide" for more information, which is available at:

http://www.actel.com/documents/install.pdf

However, in order to run Synplify for the first time, you need to run Designer before running Synplify. Please copy the andgate.adb file from the Starter Kit CD. Select Start>Program>Actel Libero IDE v5.0>Designer v5.0 to open Designer. Select File>Open and browse the andgate.adb file. This will activate the Synplify license. Then select File>Exit to close.

Hardware Installation

FlashPro Lite is required to use the ProASIC^{PLUS} Starter Kit. For software and hardware installation instructions refer the FlashPro User's Guide at:

http://www.actel.com/documents/flashproUG.pdf

1. If the user wants to use Verilog, he or she can follow the design steps but needs to write his or her own code.

Testing the Evaluation Board

If the evaluation board is shipped directly from Actel, it contains a test program that determines if the board works properly.

To test the evaluation board:

1. **Connect the power supply to the board.**
2. **Turn on the ON/OFF switch.**
3. **Perform all the actions described in** Table 3-1**.** For locations of the switches mentioned in Table 3-1, refer to Figure 2-1 on page 9.

Figure 3-1. Libero 5.0 Installation

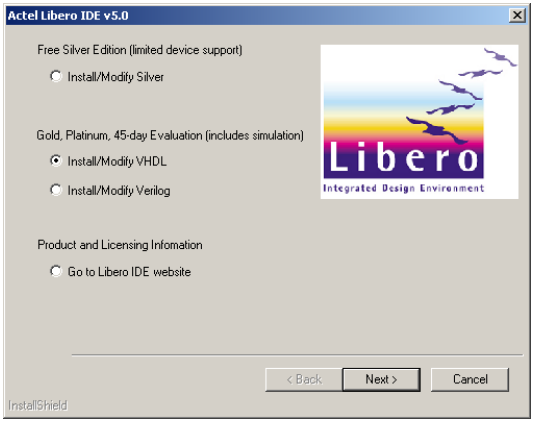


Table 3-1. Evaluation Board

Action	Result	Pass/Fail
Press PB1 multiple times, but not too quickly	Count sequence should be visible on the LEDs	Pass
Press and hold SW1	All LEDs are unlit	Pass
Press and hold SW2	All LEDs are lit	Pass

Table 3-1. Evaluation Board

Action	Result	Pass/Fail
Press and hold SW3	Count sequence runs while you hold the switch	Pass
Press and hold SW4	LED is lit/unlit alternately in a 10101010 pattern	Pass
Press any two switches simultaneously	Creates a 00110011 pattern	Pass

Programming the Test file

To retest the evaluation board at any time, use the test program to reprogram the board. Use the *test.stp* STAPL file or the *test.bit* bitstream file. These files are included on the Starter Kit CD.

This design is currently implemented for the APA075 package device. For a device of a different size, it is possible to recompile the design into other device sizes. For information about retargeting the device, refer to the *Designer User's Guide* at http://www.actel.com/documents/designerUG.pdf. The design files are available under actelprj/eval in the Starter Kit CD.

For instructions on programming the device using FlashPro Lite, refer to the *FlashPro User's Guide* at:

http://www.actel.com/documents/flashproUG.pdf

4

Actel VHDL APA Design Flow

This chapter introduces the design flow for VHDL using the Actel Libero IDE software suite. This chapter also briefly describes how to use the software tools and provides information about the sample design. Figure 4-1 shows the VHDL-based design flow.

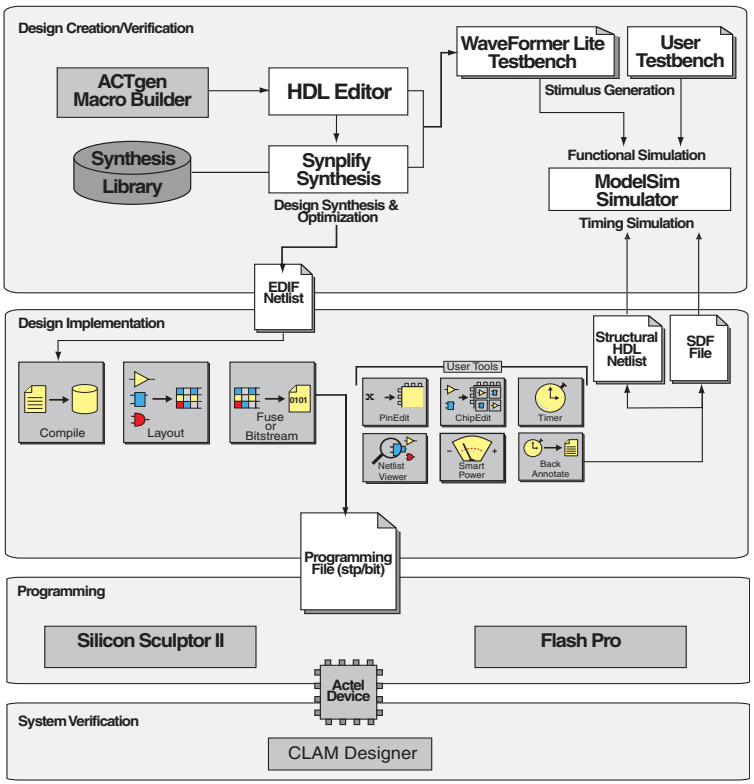


Figure 4-1. VHDL-Based Design Flow

The Libero IDE design flow has four main components:

- Design Entry
- Design Implementation
- Programming

Design Entry

Design entry consists of capturing a schematic representation of the design and performing functional simulations with a test bench.

Design Capture

For schematic capture, Libero uses ViewDraw for Actel, which includes a schematic editor. The schematic editor provides a graphical entry method to capture designs. ViewDraw for Actel is the Libero integrated schematic entry vehicle, supporting mixed mode entry in which HDL blocks and schematic symbols can be mixed.

The ViewDraw *wir* file is automatically created after using the *Save + Check* command in ViewDraw. This file is used to create the structural HDL netlist.

For more information on using ViewDraw for Actel, refer to the *Libero User's Guide* at http://www.actel.com/documents/liberoUG.pdf.

Adding ACTgen Macros

Use the ACTgen Macro Builder to instantly create customized macros and then use ViewDraw to add these macros to a schematic. Alternatively, add the ACTgen Macros in the HDL file.

Creating and Adding Symbols for HDL Files

Schematic users can encapsulate a HDL block into a block symbol.

To create a symbol:

1. **Right-click the block in the Design Hierarchy window of Libero IDE.**
2. **Click Create Symbol.** Libero IDE generates a symbol for the selected HDL block.

The macro is accessible from the components list in ViewDraw for Actel.

Test Bench Generation

It is necessary to create a test bench and associate it with a project in order to run a simulation. WaveFormer Lite from SynaptiCAD is the Libero IDE integrated test bench generator. WaveFormer Lite fits perfectly into the Libero design environment, automatically extracting signal information from HDL design files, and producing HDL test bench code that can be used with any standard VHDL or Verilog simulator.

WaveFormer Lite generates VHDL and Verilog test benches from drawn waveforms.

Pre-Synthesis Simulation

Functional simulation verifies that the logic of a design is functionally correct. Simulation is performed using the Libero integrated simulator, ModelSim for Actel. ModelSim for Actel is a custom edition of ModelSimPE that is integrated into the Libero design environment. ModelSim for Actel is an OEM edition of Model Technology Incorporated's (MTI) tools. ModelSim for Actel supports VHDL or Verilog, but it can only simulate one language at a time. It only works with Actel libraries and is supported by Actel.

Synthesis & Netlist Generation

After entering the design source, synthesize it to generate a netlist. Synthesis transforms the behavioral HDL source into a gate-level netlist and optimizes the design for a target technology.

For more detailed information on the above topics, refer to the *Libero User's Guide* at http://www.actel.com/documents/liberoUG.pdf.

Design Implementation

During design implementation, Actel's Designer places-and-routes the design.

Place-and-Route

Start Designer from Libero IDE to place-and-route the design.

Timing Simulation

Perform timing simulation on the design after place-and-route in Designer. Timing simulation requires information extracted and back-annotated from Designer.

Optional Tools

The tools listed in Table 4-1 provide optional functions that are not required in a basic design. Use these tools to perform static timing analysis, power analysis, customize I/O placements and attributes, and view the netlist. After place-and-route, perform the post-layout (timing) simulation.

Table 4-1. Designer's User Tools

Designer User Tools	User Tool Function
Timer	Static timing analysis
SmartPower	Power analysis
Netlist Viewer	View your netlist and trace paths
PinEditor	Customize I/O placements
ChipPlanner	Customize I/O and logic macro placements. Help to do floorplan on the design.
I/O Attribute Editor	Customize I/O attribute

For more information on the tools described in the above section, refer to the *Designer User's Guide* at http://www.actel.com/documents/designerUG.pdf.

Programming

Program the device with programming software and hardware from Actel or a supported 3rd party programming system. Refer to the *Designer User's Guide*, *Silicon Sculptor User's Guide*, and *FlashPro User's Guide* for information about programming an Actel device.

These guides can be found at:

http://www.actel.com/techdocs/manuals/default.asp

System Verification

Use the CLAM diagnostic tool, available from FS^2, to perform system verification on a programmed device. Refer to *Technical Data For CLAM® System for Actel FPGA Devices* for information about using CLAM. This guide can be found at:

http://www.actel.com/documents/CLAMActel.pdf

5 Quick Start Tutorial

This tutorial illustrates a simple basic VHDL design for an APA Evaluation Board. The design is targeted at the Actel ProASIC^{PLUS} family. To show the design in its simplest form, a simple andgate design is created in Actel's Libero IDE 5.0. The steps involved are:

Step 1 – Create a New Project

This step uses the Libero IDE HDL Editor to enter an Actel VHDL design.

To create the VHDL project:

1. **Start Libero IDE by double-clicking the Actel Libero IDE icon on the desktop.**

2. **From the File menu, select** *New Project***.** The New Project dialog box is displayed, as shown in Figure 5-1.

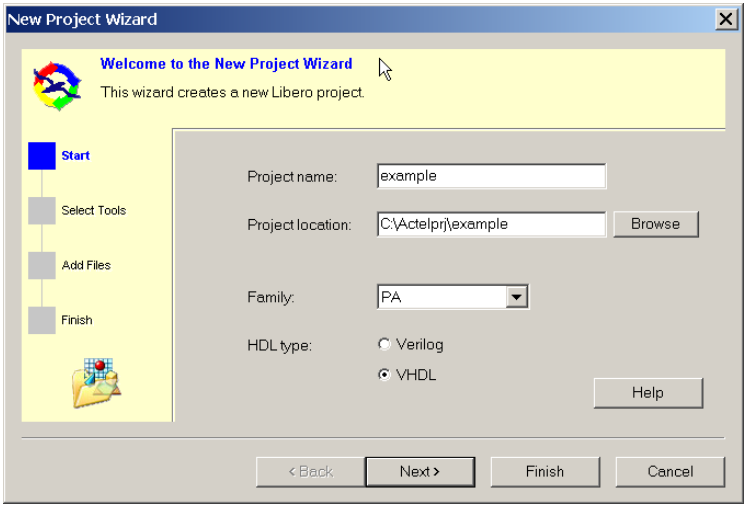


Figure 5-1. New Project Dialog Box

3. **Enter** *example* **in the Project Name field.**
4. **In the Project Location field, click *Browse* to navigate to C:\Actelprj.**
5. **Select** *PA* **from the Family drop-down list.**
6. **Check the** *VHDL* **radio button in the HDL type field.**
7. **Click *Finish*.** The project "example" is created and opened in the Libero IDE.

8. **From the File menu, click *New*.** This opens the New dialog box, as shown in Figure 5-2.

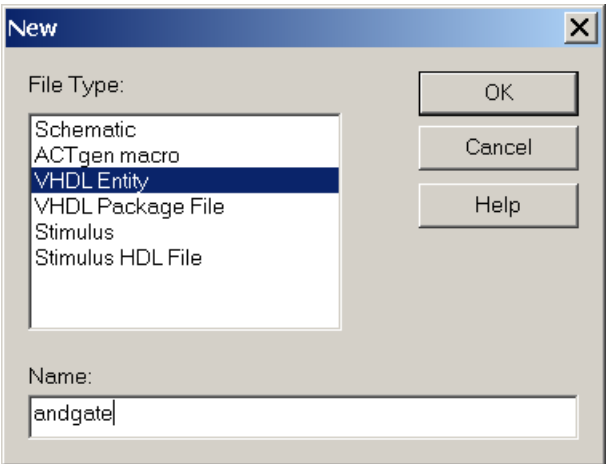


Figure 5-2. New File Dialog Box

9. **Select *VHDL Entity* in the File Type field, enter *andgate* in the Name field and click *OK*.** The HDL Editor opens.

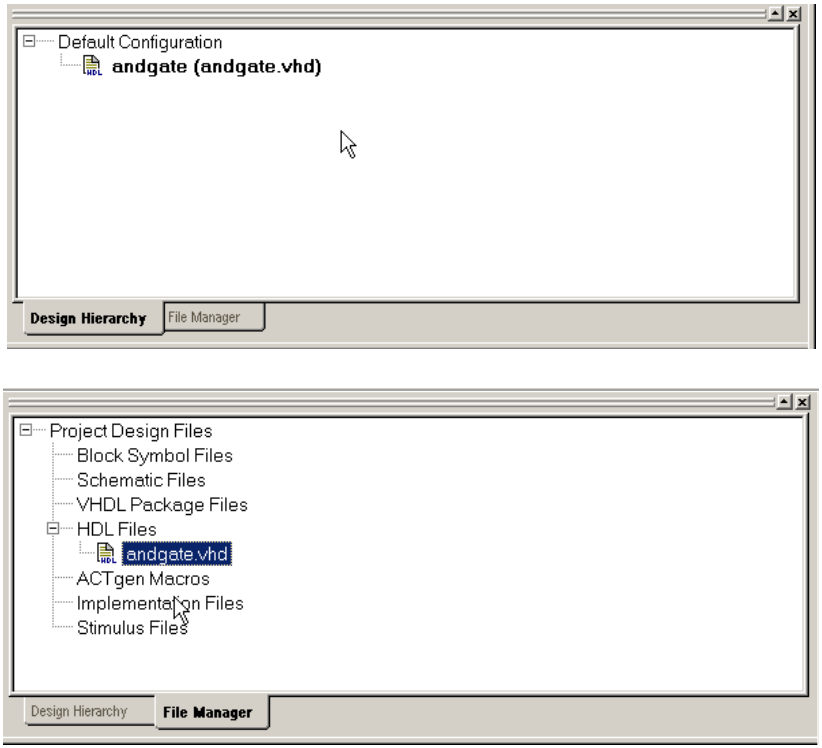
10. **Enter the following VHDL file, or if this document is open in an electronic form, cut and paste it from this document.**

```
-- AND Gate Tutorial for APA Evaluation Board
LIBRARY ieee;
USE ieee.std_logic_1164. ALL;

ENTITY andgate is
port (A, B : in std_logic;-- Data Inputs
OUTPUT : out std_logic); -- Output= A AND B
end andgate;

architecture behaviour of andgate is

begin

OUTPUT <= A AND B;

end behaviour;
```

11. **From the File menu, click *Save*.** The design file "andgate" will now appear under the Design Hierarchy tab in Libero IDE. The file name

"andgate.vhd' is listed under HDL files in the File Manager tab in the Libero IDE, as shown in Figure 5-3.

Figure 5-3. Design Hierarchy Tab and File Manager Tab



12. **Click the File Manager tab.**

13. **Right-click on** *andgate.vhd* **and run "check HDL".** This checks the syntax of the *andgate.vhd* file. Before moving to the next section, please modify the code if any errors are visible.

Step 2 – Perform a Pre-synthesis Simulation

The next step is simulating the RTL description of the design. First, use WaveFormer Lite to create a stimulus for the design and then generate a test bench for the design.

Creating Stimulus Using WaveFormer Lite

WaveFormer Lite generates VHDL test benches from drawn waveforms. There are three basic steps for creating test benches using WaveFormer Lite and the Actel Libero IDE software:

1. Import Signal Information
2. Drawing Waveforms
3. Export the Test Bench

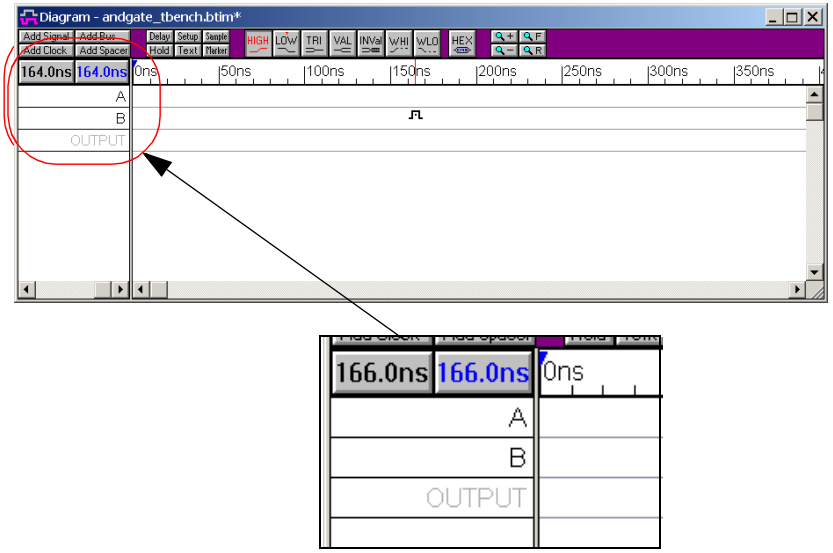
Import Signal Information

To launch WaveFormer Lite and import signal information into it:

1. **Double-click the WaveForm Lite icon in the Libero IDE, or right-click the** *andgate* **file in the Design Hierarchy tab and select** *Create*

Stimulus. WaveFormer Lite launches, with the port signals appearing in the Diagram window, as shown in Figure 5-4.

Figure 5-4. WaveFormer Lite Timing Diagram Window



The andgate design contains the following signals:

- A Input signal
- B Input signal
- OUTPUT Output Signal

Drawing Waveforms

To draw a Waveform:

The state buttons are the buttons with the waveforms drawn on their face: HIGH, LOW, TRIstate, VALid, INValid, WHI weak high, and WLO weak low, as shown in Figure 5-5.

Figure 5-5. State Buttons

When a state button is activated, it is pushed in and colored red. The active state is the type of waveform that is drawn next. To activate a state button, click on it.

The state buttons automatically toggle between the two most recently activated states. The state with the small red "T" above the name will be the toggle state. The initial activated state is HIGH and the initial toggle state is LOW.

Signal edges are automatically aligned to the closest edge grid when signals are drawn using the mouse. Control the edge grid from the Options > *Grid Settings* menu item.

1. **Select the High state and place the mouse cursor inside the Diagram window at the same vertical row as the signal name.**
2. **Click the left mouse button.** This draws a waveform from the end of the signal to the mouse cursor. The red state button on the button bar determines the type of waveform drawn. The cursor shape also mirrors the red state button.
3. **Move the mouse to the right and click again to draw another segment.**

To copy waveforms:

It is possible to copy and paste sections of waveforms onto (overwrite) or into (insert) any signal in the diagram. To copy and paste waveform sections:

1. **Select the names of the required signals.** If no signals are selected, the Block Copy command selects all the signals in the diagram.

2. **Select the Edit > Block Copy Waveforms menu option.** This opens the Block Copy Waveforms dialog box with the selected signals displayed in the Change Waveform Destination list box.

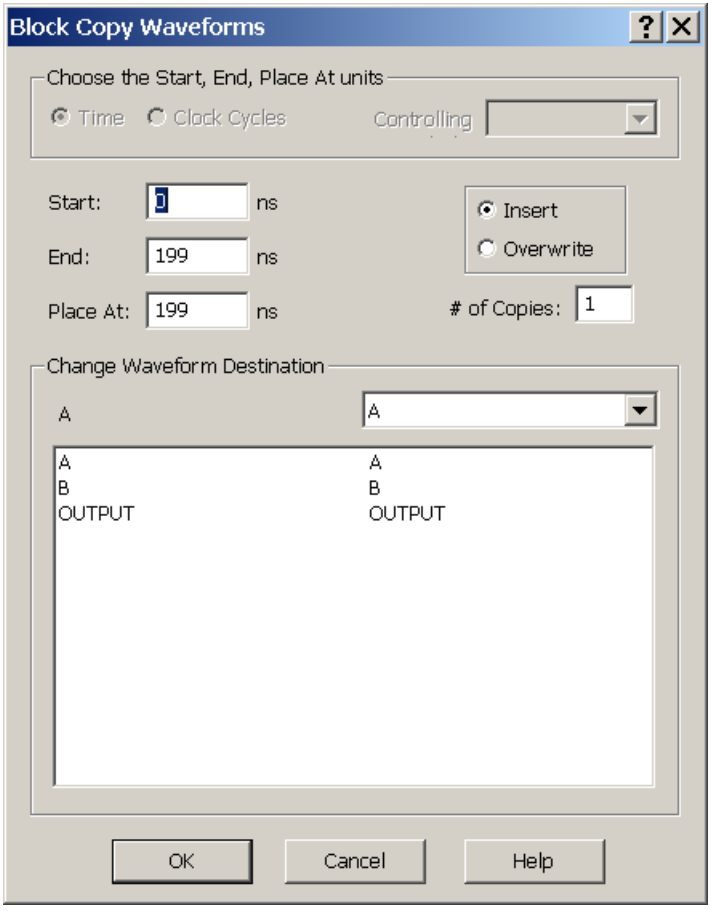


Figure 5-6. Block Copy Waveforms Dialog Box

3. **In the dialog, enter the values that define the copy and paste.**

   Select either Time or Clock cycle for the base units of the dialog. Remember:

   - When copying only signals (no clocks), time is the default base unit of the dialog.
   - When copying part of a clock, it is best to choose a clock cycles base unit and choose the copied clock as the reference clock.
   - If time is selected when copying clocks, the (end_time - start_time) must equal an integral number of clock periods, and the place_at time must be at the same clock period offset as the start_time.
   - *Start* and *End* define the times of the block copy.
   - *Place At* is the time at which the block will be pasted.
   - The *Insert* and *Overwrite* radio buttons determine whether the paste block is inserted into the existing waveforms or overwrites those waveforms.
   - The list box at the bottom of the dialog determines which signal the copied waveforms will be pasted into.

   To change this mapping:

   - Select a line in the list box.

     This places the destination signal in the drop-down list box on top of the list box.

   - Select another signal from the drop-down list box.

     Each destination signal can be used only once per copy.

   - Click *OK* to complete the copy and paste operation.

Export the Test Bench

In this step a stimulus file is created for the design and a test bench is generated using WaveFormer Lite. After exporting the testbench, perform a pre-synthesis simulation using ModelSim.

To Create a Stimulus File and Generate a VHDL Testbench:

In this step, a design stimulus file is created using WaveFormer Lite. Following the instructions in the previous sections, define values for the A input signal (A), the B input signal (B), and the output signal (OUTPUT).

1. **Following the instructions on the previous pages, create waveforms for A and B, as described below:**

Table 5-1.

A –	low 0nS – 100 ns
	high 100 nS – 1 us
B –	low 0nS – 300 ns
	high 300 nS – 330 ns
	low 330 nS – 1 us

This creates the waveform shown in Figure 5-7.

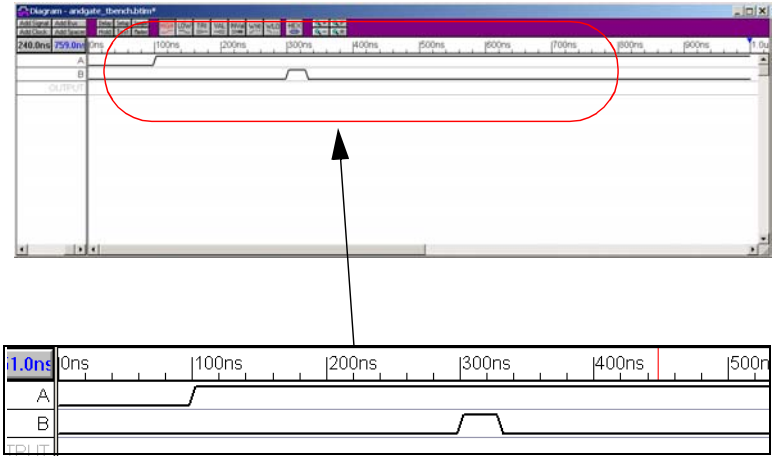


Figure 5-7. WaveForm Timing diagram

2. **After successfully creating the waveforms, select** *Save As* **from the File menu. In the Save As dialog box, enter** *andgate_stim.btim* **as the file name and click** *Save*.

3. **After saving the timing diagram file, select** *Export Timing Diagram As* **from the Export menu.**

4. **Select** *"VHDL w/ Top Level Test Bench (*vhd)"* **in Files of Type and enter** *andgate_stim.vhd* **for the file name, as shown in** Figure 5-8.

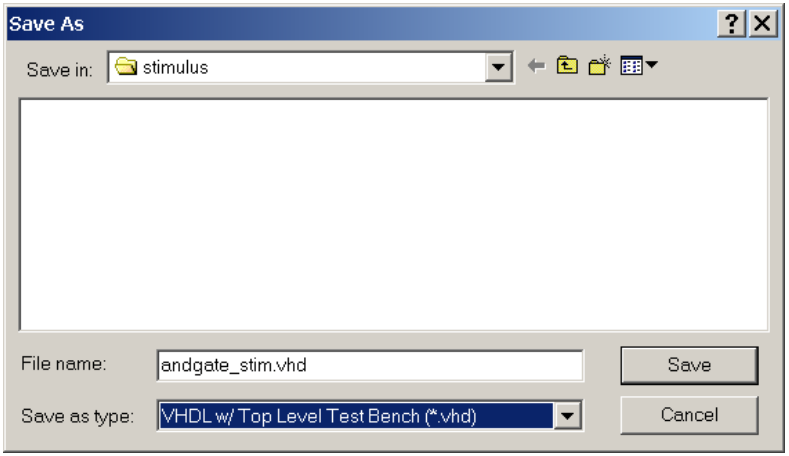


Figure 5-8. andgate_stim.vhd

The WaveFormer Lite Report window displays the VHDL testbench with a component declaration and instantiation inside.

5. **Exit WaveFormer Lite (File > Exit).** The Libero IDE File Manager tab displays the stimulus files.

   The design is ready to simulate under ModelSim.

To create a testbench using HDL editor:

Alternatively, create a testbench using the HDL editor. To create a stimulus file with the HDL Editor:

1. **From the File menu, select** *New*. This opens the New File dialog box.

2. **Select** *Stimulus HDL file* **from the File Type list, enter** *andgate_stim* **for the name, and click** *OK*. The file opens in the HDL Editor.

3. **Create the VHDL testbench and save it.**

Note: Please use "testbench" as the entity name and follow Libero naming convention. See Libero User's Guide for more information

Pre-Synthesis Simulation

Once the test bench is generated, use ModelSim to perform a pre-synthesis simulation.

To perform a pre-synthesis simulation:

1. **Select a stimulus file. Right-click andgate in the Libero IDE Design Hierarchy tab and select** *"Select Stimulus"***, as shown in** Figure 5-9**.**

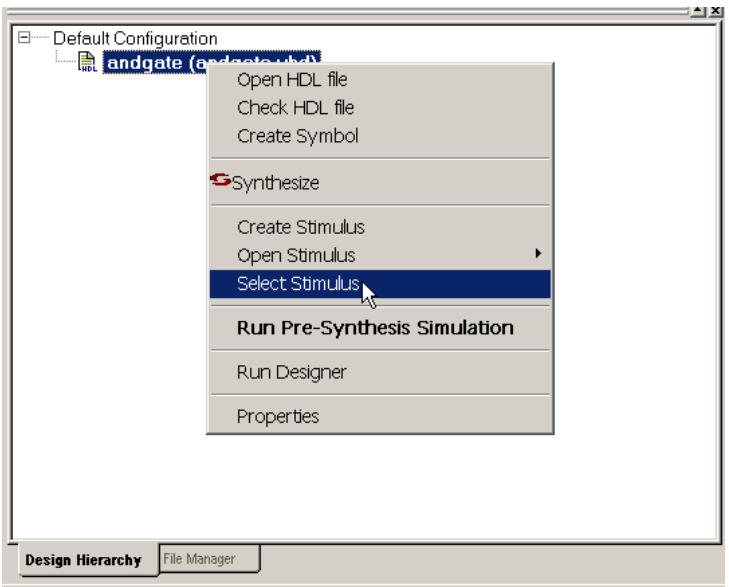


Figure 5-9. Selecting a Stimulus File

The Select Stimulus dialog box shown in Figure 5-10 appears.

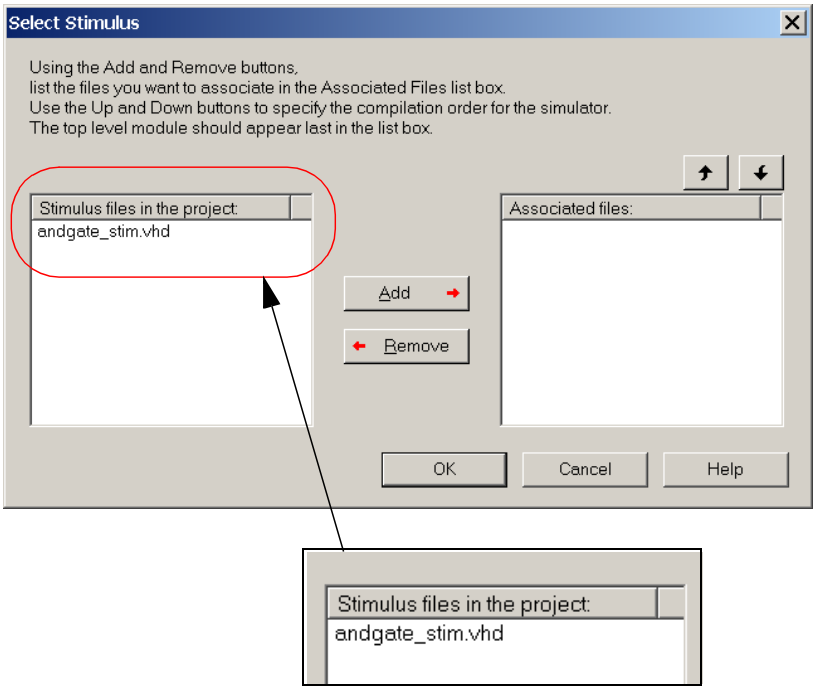


Figure 5-10. Select Stimulus Dialog Box

2. **Select *andgate_stim.vhd* in the Project List box and click Add to add the file to the Associated Files list.**

3. **Click OK.** A check mark appears next to Waveformer Lite in the Process window, as shown in Figure 5-11.

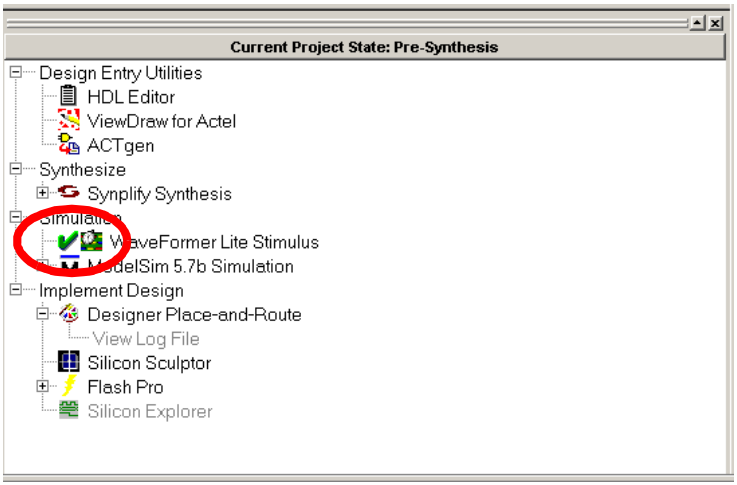


Figure 5-11. Check Mark in Waveformer Lite

4. **Double-click the ModelSim simulation icon in the Libero IDE Process window, or right-click** *andgate* **in the Libero IDE Design Hierarchy tab and select** *Run Pre-synthesis Simulation,* **as shown in** Figure 5-12**.**

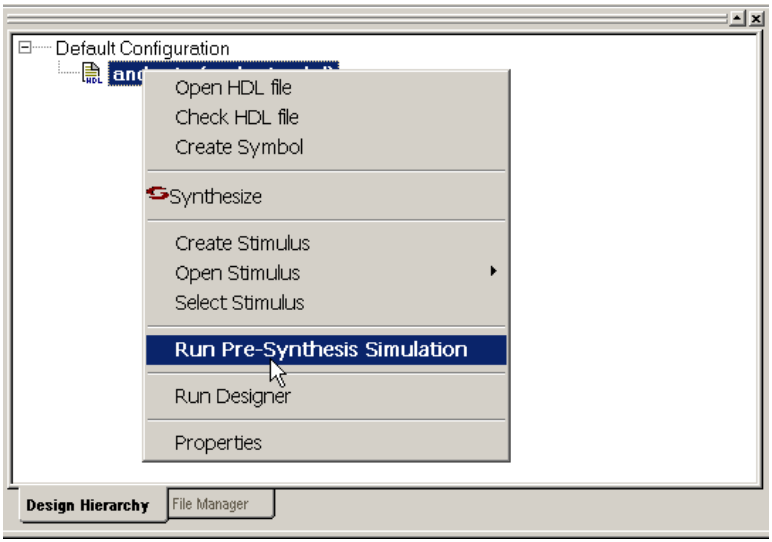


Figure 5-12. Run Pre-Synthesis Simulation

5. The ModelSim VHDL simulator opens and compiles the source files, as shown in Figure 5-13.

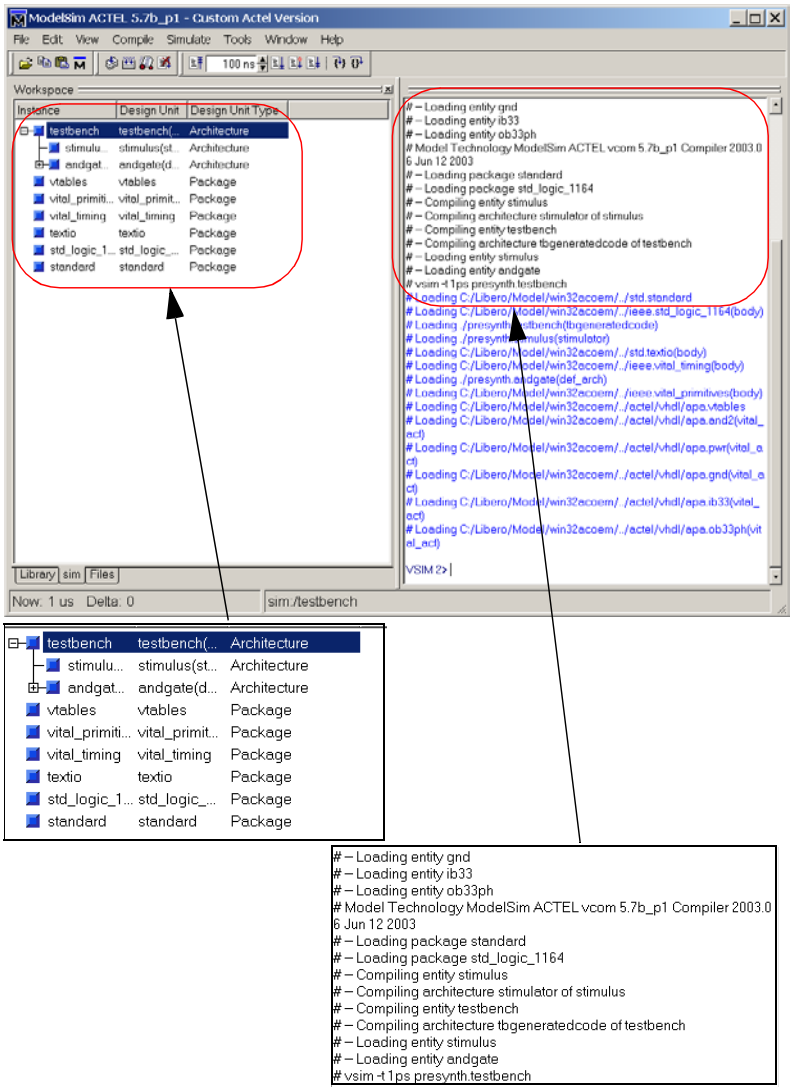


Figure 5-13. ModelSim Main Window

Once the compilation completes, the simulator simulates for the default time period of 1000ns and a Wave window, shown in Figure 5-14, opens to display the simulation results. Scroll in the Wave window to verify that the design functions properly.

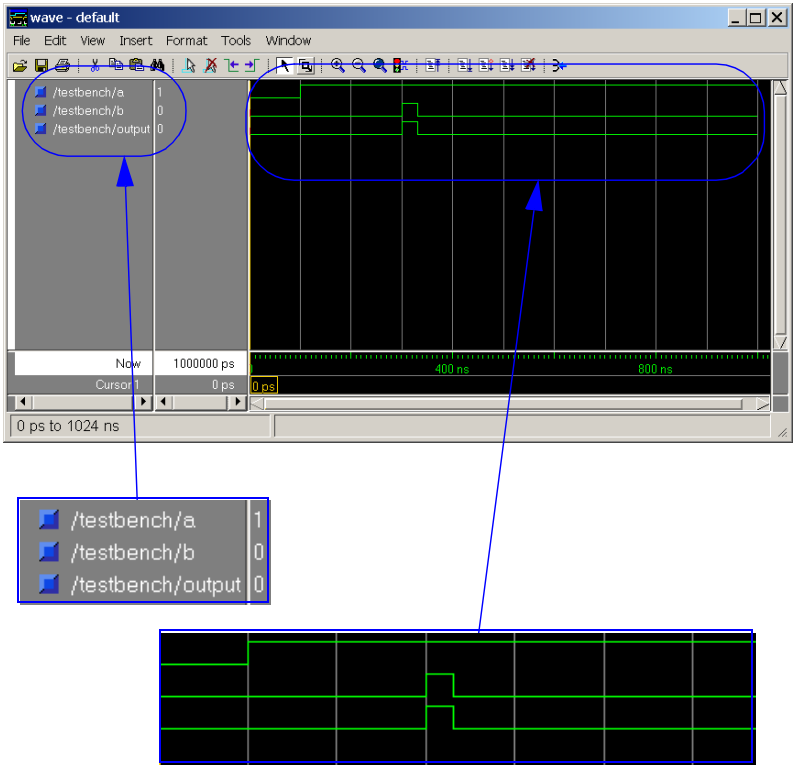


Figure 5-14. ModelSim Wave Window

6. **In the Modelsim window, select File > Quit to close the window.**

Step 3 – Synthesize the Design in Synplify

The next step is generating an EDIF netlist by synthesizing the design in Synplify. For HDL designs, Libero IDE launches and loads Synplicity's Synplify synthesizer with the appropriate design files.

To create an EDIF netlist for the design using Synplify:

1. **In the Libero IDE, double-click the Synplify Synthesis icon in the Libero IDE process window or right-click the *andgate* file under the Design Hierarchy tab and select *Synthesize*.** This launches the Synplify synthesis tool with the appropriate design files, as shown in Figure 5-15.

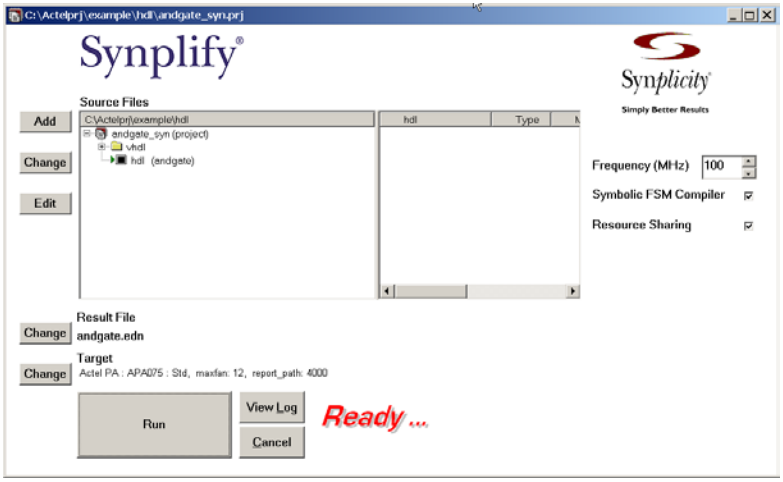


Figure 5-15. Synplify

2. **From the Project menu, select** *Implementation Options***.** The Options for Implementation dialog box is displayed, as shown in Figure 5-16.

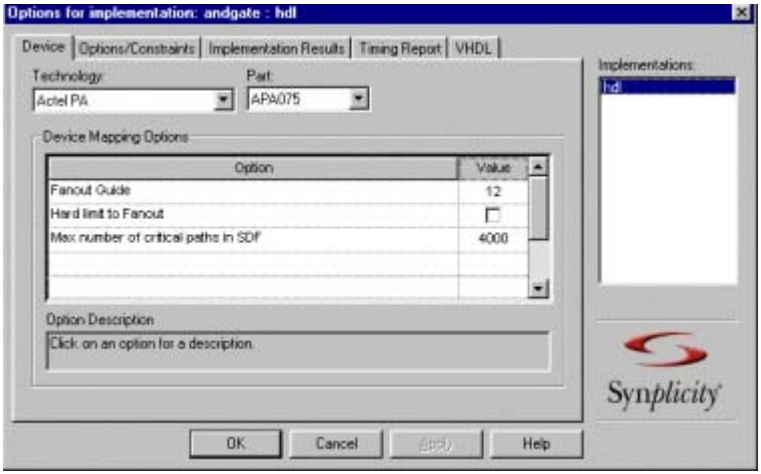


Figure 5-16. Options for Implementation Dialog Box

3. **Set the following in the dialog box:**

   - Technology: Actel PA (Set by Libero IDE)
   - Part: APA075
   - Fanout Guide: 12 (Default)
   - Hard Limit to Fanout; Off (Default). This refers to the fanout limit.

   Accept the default values for each of the other tabs in the Options for Implementation dialog box and click *OK*.

4. **In the Synplify main window, click** *Run***.** Synplify compiles and synthesizes the design into a netlist called *andgate.edn*. The resulting *andgate.edn* file is then automatically translated by Libero into a VHDL netlist called *andgate.vhd*.

   The resultant EDIF and VHDL files are displayed under the Implementation Files in the File Manager tab of Libero IDE.

   Note: If any errors appear after clicking the **Run** button, edit the file using the Synplify editor. To edit the file, double-click the file name in the

Synplify window. Any changes made here are saved to the original design file in Libero IDE.

5. **Save and close Synplify.** From the File menu, click *Exit* to close Synplify. Click *Yes* to save any settings made to the *andgate.prj* in Synplify.

Step 4 – Perform a Post-Synthesis Simulation

The next step is simulating the VHDL netlist of the andgate using the VHDL testbench created in "To Create a Stimulus File and Generate a VHDL Testbench:" on page 33.

1. **Click the ModelSim Simulation icon in the Libero IDE Process window, or right-click the** *andgate* **file in the Design Hierarchy tab and select** *Run Post-Synthesis Simulation***.** This launches the ModelSim Simulator which compiles the source file and test bench.

   Once the compilation completes, the simulator runs for 1000 ns and a Wave window opens to display the simulation results.

2. **Scroll in the Wave window to verify that the andgate works correctly.** Use the zoom buttons to zoom in and out as necessary.

Step 5 – Implement the Design with Designer

After creating and testing the design, the next phase is implementing the Design using the Actel Designer Software.

1. **Double-click the** *Designer Place and Route* **icon in the Libero IDE Process window, or right-click the mouse on andgate in the Design Hierarchy tab of the Design Explorer Window, and select *Run Designer*.** Actel's Designer application opens and the design file is read in.

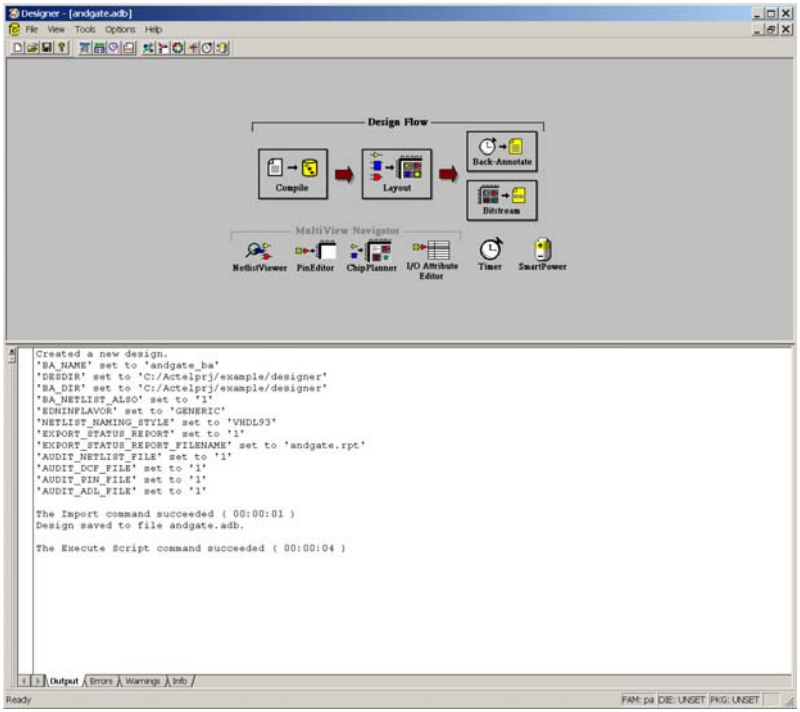


Figure 5-17. Designer

2. Compile the design.

From the Tools menu, select *Device Selection*. This opens the Device Selection Wizard shown in Figure 5-18.

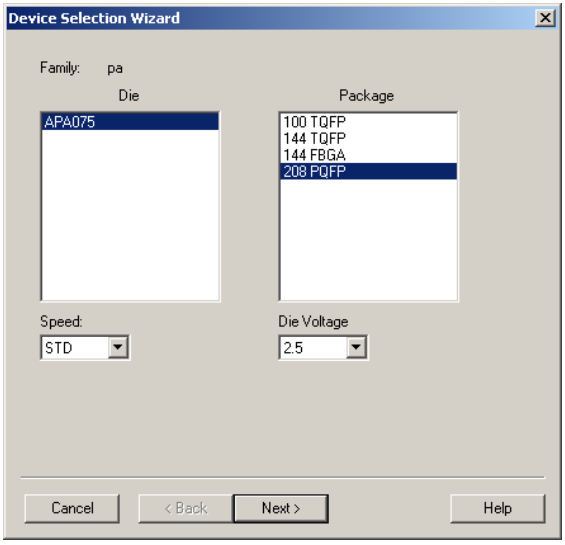


Figure 5-18. Device Selection Wizard

Select *APA075* in the Die field and select *208 PQFP* in the package field. Accept the default speed grade and die voltage and click *Next*.

Complete the remaining fields and click *Finish*. Double-click the Compile icon.

Designer compiles the design and shows the utilization of the selected device. Also, note that the Compile icon in Designer turns green indicating that the compile has successfully completed.

3. PIN Assignment

Once the design compiles successfully, use the PinEditor tool to drag and drop the placement of pins and fix pin locations for subsequent place-and-route runs.

1.) Click the PinEditor user tool. This opens the PinEditor window inside the MultiView Navigator window..

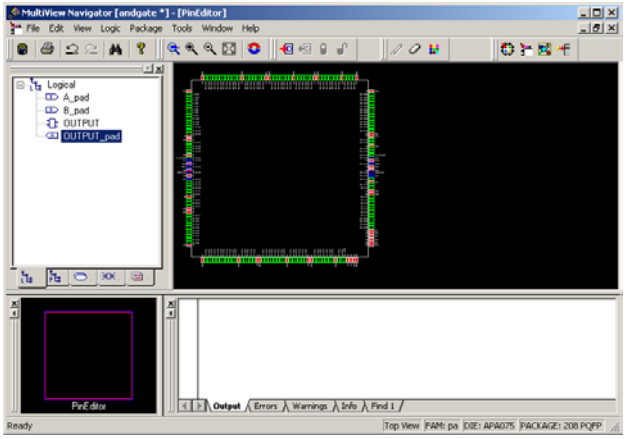
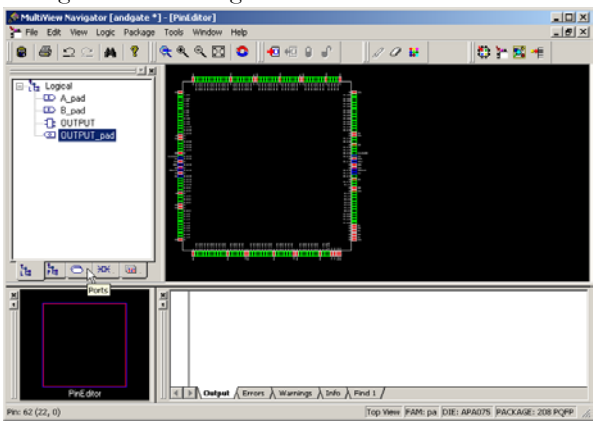


Figure 5-19. PinEdit Window

Please Follow the steps below to assign the pins:

2.) Select port tab in the MultiView Navigator window as shown in Figure 5-20 below

Figure 5-20. Selecting Port Tabs in PinEditor Window



3.) Expand the ports by selecting the "+" sign in ports tab.

4.) Drag the port to the pin location.

Assign A to pin 55, B to pin 63, and the output to pin 87, as shown in Table 5-2.

Table 5-2.Pin Assignments

Signal	Direction	PIN
A	Input	55 (SW1)
B	Input	63 (SW1)
OUTPUT	Output	87 (LED DS1)

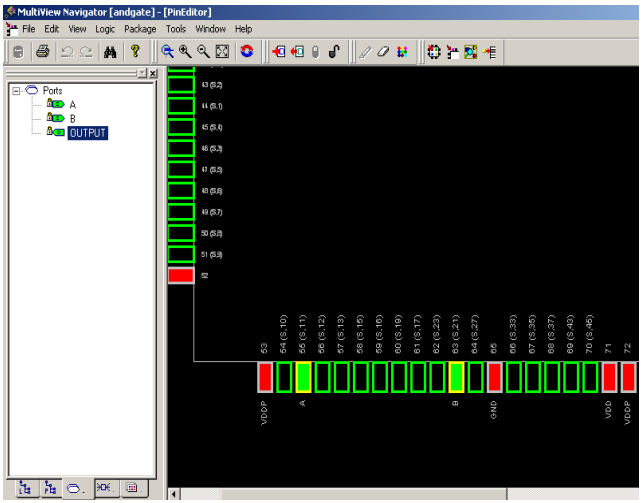


Figure 5-21. PinEdit Window With Pins Assigned

5.) Once a pin number is assigned to all of the signals, select Commit from the File menu and close the PinEdit window.

4. **(Optional) Designer User Tools.**

   After successfully compiling the design, use the Designer Tools to view pre-layout static timing analysis with Timer, set time constraints in Timer, and use ChipEdit to assign modules. Access each of these functions by clicking the required icon.

   For more information on these functions, refer to the *Designer's User Guide* and online help. For this tutorial, no changes are made to the design.

5. **Layout the Design.**

From Designer, click the Layout icon. This opens the Layout Options dialog box shown in Figure 5-22.

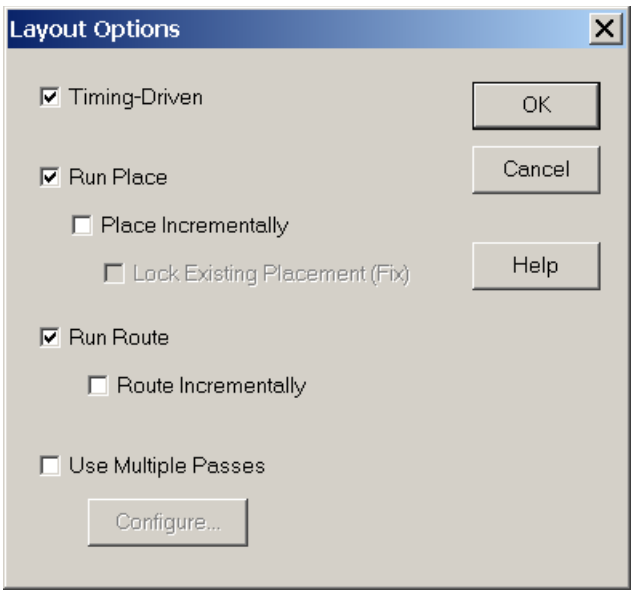


Figure 5-22. Layout Options Dialog Box

Click *OK* to accept the default layout options. This runs the placer-and-router on the design. The layout icon in designer turns green to indicate that the layout has successfully completed.

6. **Back-Annotate the design.**

   From Designer, click the Back Annotate icon. This opens the Back-Annotate dialog box shown in Figure 5-23.

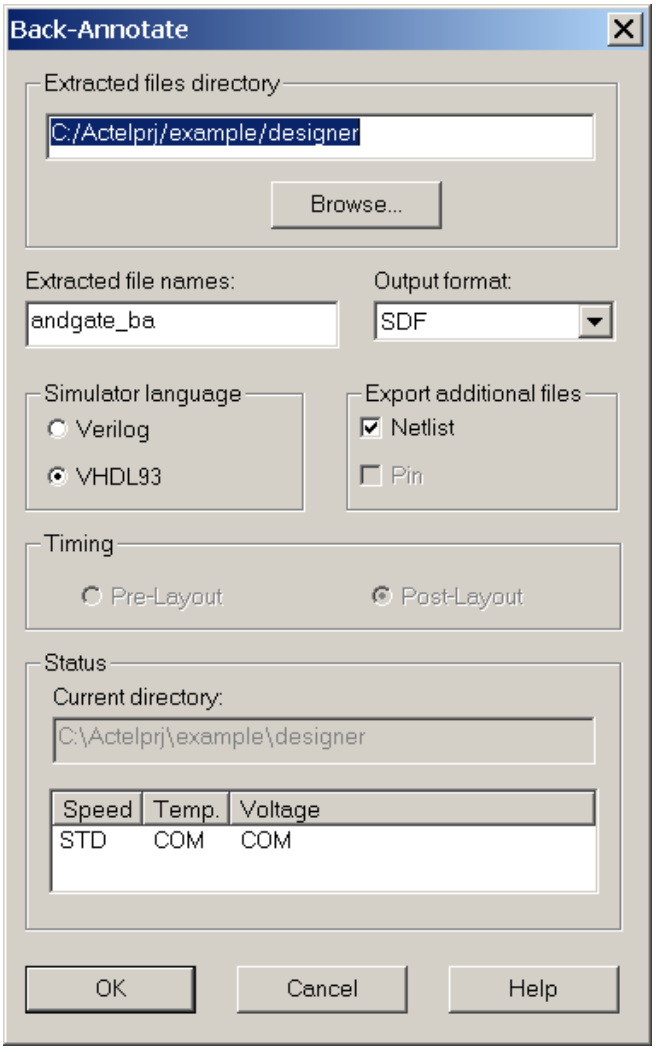


Figure 5-23. Back Annotate Dialog Box

Accept the default settings and click *OK*. The Back Annotate icon turns green.

7. **Save and close Designer.**

   From the File menu, click *Exit*. Click *Yes* to save the design before closing designer. Designer saves all the design information in a **.adb* file.

   The file *andgate.adb* appears under the Designer Files of the File Manager tab in Libero IDE. To reopen the file, right-click the file and select *Open in Designer*.

Step 6 – Perform a Timing Simulation with Back-Annotated Timing

After completing the place-and-route and back annotation of the design, perform a timing simulation with the ModelSim HDL simulator.

To perform a timing simulation:

1. **Click the ModelSim Simulation icon in the Libero IDE Process window, or right-click the *andgate* file in the Design Hierarchy tab and select *Run Post-Layout Simulation*.**

   This launches the ModelSim Simulator which compiles the back annotated VHDL netlist file and test bench.

   Once the compilation completes, the simulator runs for 1000 ns and a Wave window opens to display the simulation results.

2. **Scroll in the Wave window to verify that the andgate works correctly.**

   Use the zoom buttons to zoom in and out as necessary.

Step 7 – Generate the Programming File

This step generates the necessary file for programming the ProASIC^{PLUS} APA Evaluation Board.

1. **Right click andgate in the Design Hierarchy tab to open Designer.**
2. **Double-click the Bitstream icon in Designer, or select** *Export* **->** *Bitstream Files* **from the File menu.** This opens the Generate Programming Files: Bitstream Files dialog box, as shown in Figure 5-24.

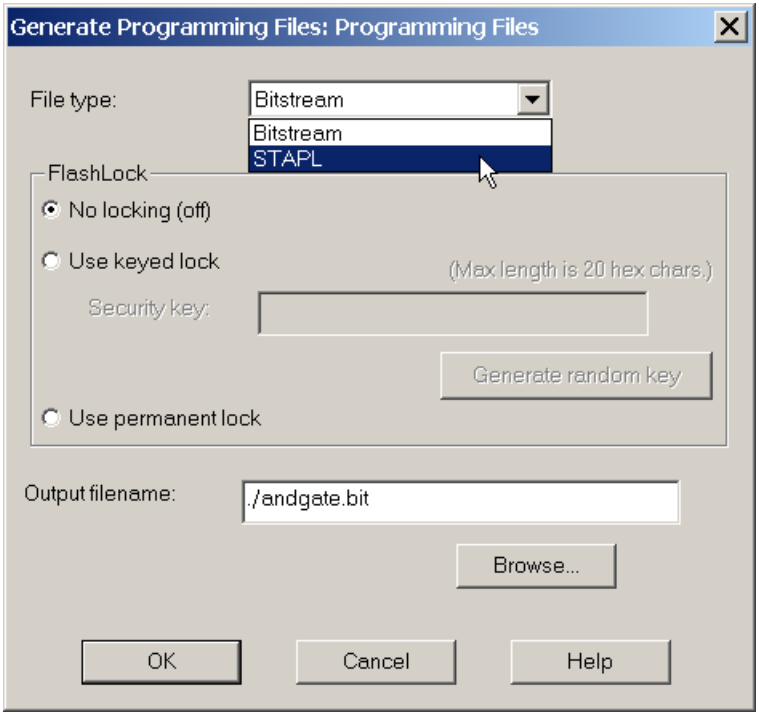


Figure 5-24. Bitstream File Dialog Box

3. **Select** *STAPL* **from the File Type drop-down list box.**
4. **Select an Output File Name.** Enter the *andgate* file name or select the *andgate* file by clicking the *Browse* button. The Bitstream file dialog box appears.

5. **Click** *OK***.** On successful completion, the Bitstream icon turns green. The programming file is saved to the Libero IDE, appearing in the File Manager under implementation files.

   Note: The STAPL file header contains the security key.

Step 8 – Program the Device

After generating the programming file, program the device using Actel's FlashPro Lite programmer.

Initial Setup

Before performing any action with the FlashPro programmer, it must be properly setup. Please properly connect the FlashPro ribbon cable with the programming header and turn on the switch.

To setup FlashPro Lite:

1. **From the File menu, click *Connect*.** The FlashPro Connect to Programmer dialog box displays, as shown in Figure 5-25.

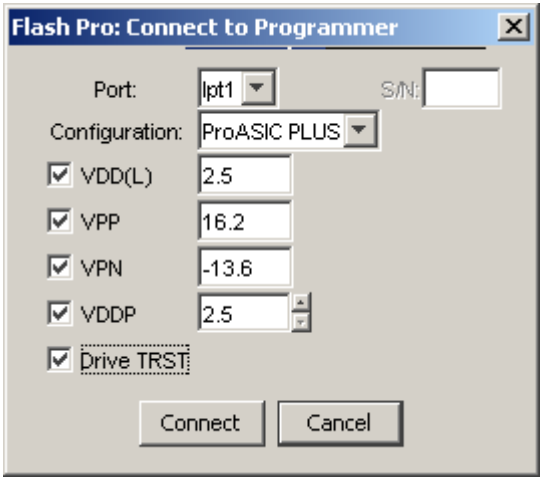


Figure 5-25. FlashPro: Connect to Programmer Dialog Box

2. **In the Port list, select the port the FlashPro programmer is connected to.**
3. **In the Configuration list, select ProASIC PLUS.** FlashPro Lite does not support ProASIC devices.
4. **(Optional) Disable voltages from the programmer if they are available on the board.**

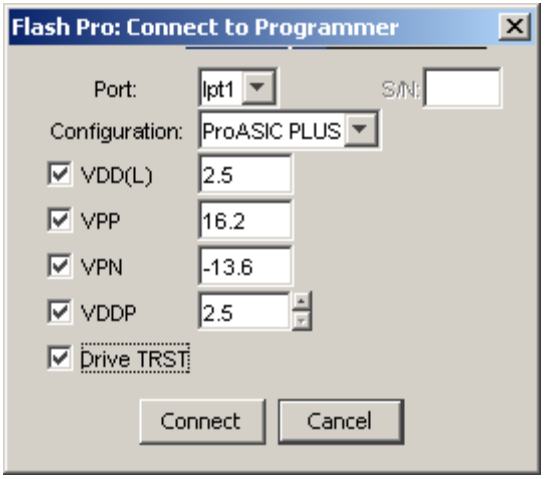


Figure 5-26. Connect to Programmer Dialog Box for ProASIC^{PLUS} Devices

Note: To power-up the device from the board power supply, please deselect VDD(L) and VDDP. VPP and VPN are required during programming only and are supplied by the FlashPro programmer. FlashPro Lite only supports ProASIC^{PLUS} devices as shown in the

FlashPro Lite Log window in Figure 5-27. Use FlashPro to program ProASIC devices.

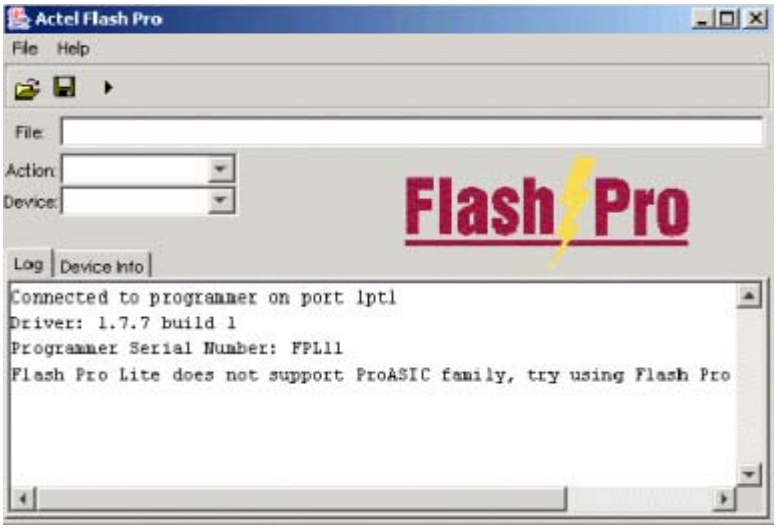


Figure 5-27. FlashPro Lite Log Window

5. **Click *Connect*.** A successful connect, or any errors, appear in the Log window, as shown in Figure 5-28.

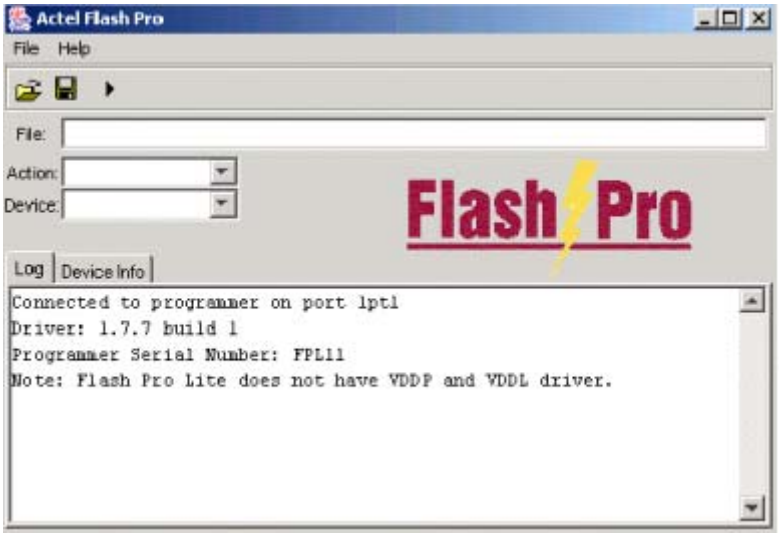


Figure 5-28. FlashPro Lite Successful Connection

Note: FlashPro Lite does not have VDDP and VDD drivers.

Analyze Chain and Device Selection

To analyze the chain and select the device:

1. **From the File menu, click *Analyze Chain*.** Chain details appear in the Log window, as shown in Figure 5-29. If any failures appear, refer to the error and troubleshooting section of the *FlashPro User's Guide* at:

   http://www.actel.com/documents/flashproUG.pdf

Figure 5-29. FlashPro: Analyzing Chain

2. **Select the APA 075 device from the Device list**. If only one device is present in the chain, performing Analyze Chain selects that device automatically from the Device list.

Loading the STAPL File

FlashPro Lite programmer uses a STAPL (*.stp) file to program the device.

To load the STAPL file:

1. **Click the *Open File* button in the toolbar, or from the File menu, click "Open STAPL file".**

The Open dialog box appears, as shown in Figure 5-30.

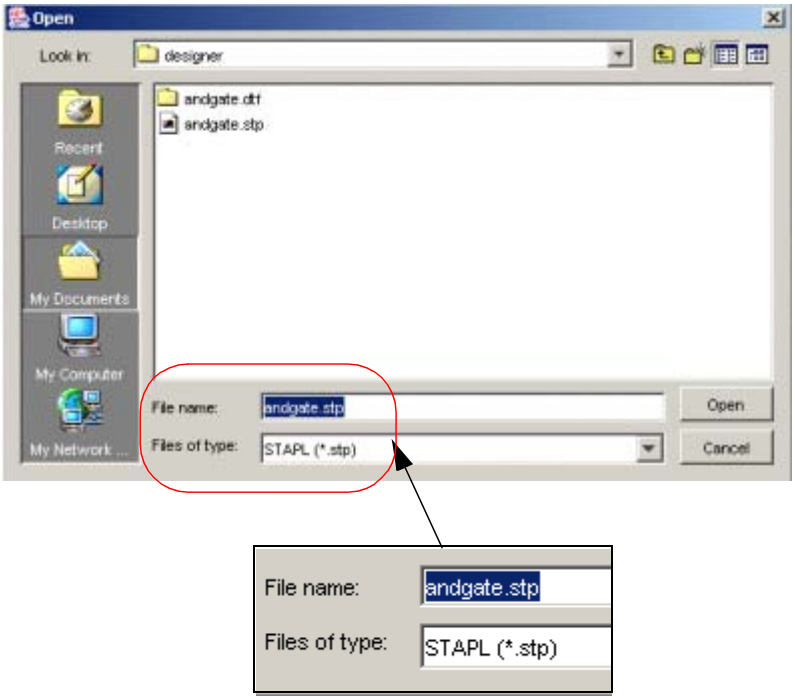


Figure 5-30. Open Dialog Box

2. **Browse to the root folder of the project, select the STAPL file, and click *Open*.** The FlashPro software loads the file. The FlashPro Log window displays a message indicating that the software has successfully loaded, as shown in Figure 5-31.

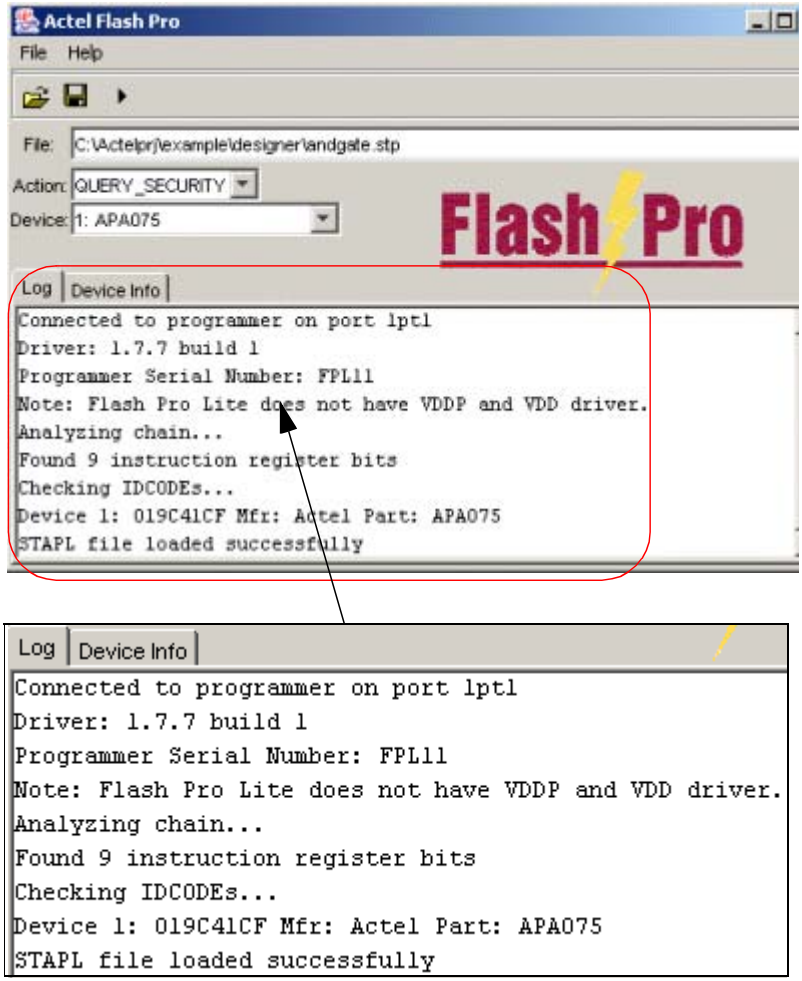


Figure 5-31. STAPL file loaded successfully

Selecting an Action

After loading the STAPL file, select an action from the Action list. See Table 5-3 for a definition of each action.

Table 5-3.Action Options

Option	Action
QUERY_SECURITY	Checks for security feature. If the device is programmed with the security feature, then this command exists with Read inhibit:1 Write inhibit:1. If the security feature is not present, the values are Read inhibit:0 Write inhibit 0.
ERASE	Erases the device.
READ_IDCODE	Reads the device ID code.
VERIFY	Verifies whether the device was programmed with the loaded STPL file. If the wrong STPL file is loaded, an Exit 11 result appears in the log window. A successful operation results in Exit 0. This command resembles the checksum command of anti-fuse product's programming.
PROGRAM	Programs the device.
DEVICE_INFO	Displays the serial number of the device, the Design Name that is programmed into the device, and the checksum that is programmed into the device.

Programming the Device

To program the device:

1. **In the Action list, select *PROGRAM*.**
2. **In the Device list, select the APA 075 device.**
3. **Click the *Execute* button in the toolbar.**

The Execute Action dialog box appears, as shown in Figure 5-32.

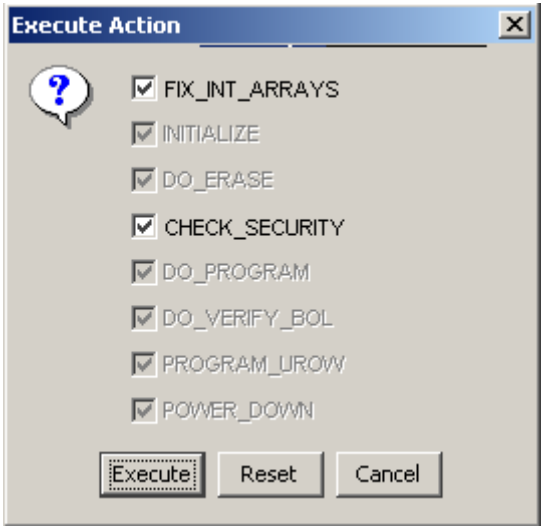


Figure 5-32. Execute Action Dialog Box

All the steps of the programming sequence are listed. Optional steps appear in bold. Grayed out options are required for programming and cannot be changed.

4. **Make the required selections and click *Execute* to start programming.** The progress of the programming action displays in the Log window. The message 'Exit 0' indicates that the device has successfully been programed, as shown in Figure 5-33.

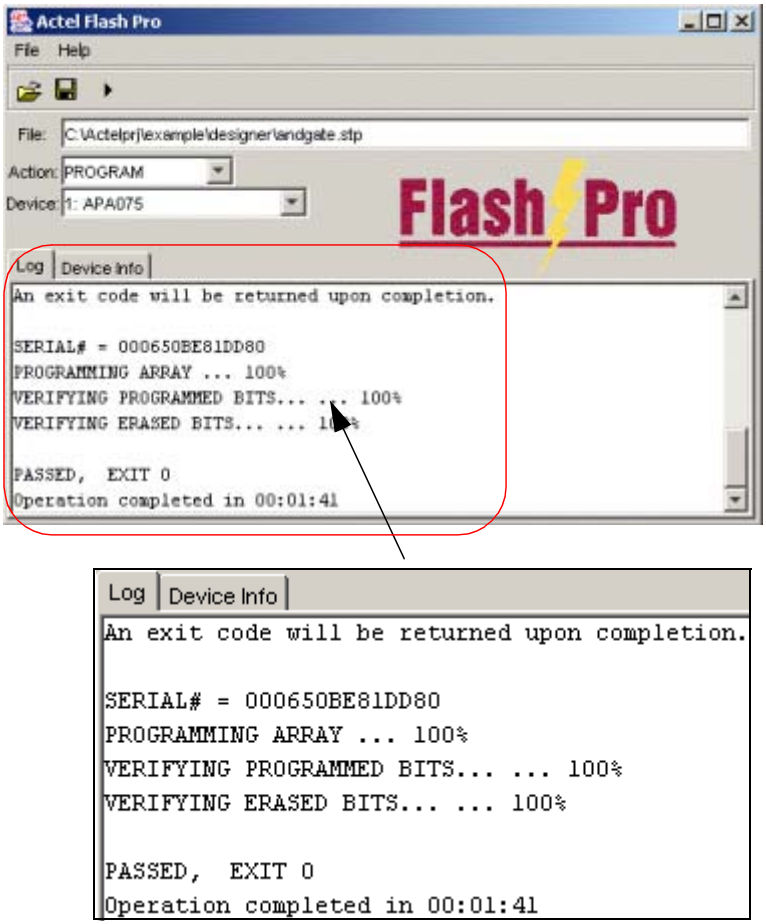


Figure 5-33. Successfully Programmed Device

Note: Do not interrupt the programming sequence, it may damage the device or programmer.

If you encounter any failures, please refer to the troubleshooting section of the *FlashPro User's Guide*.

Check Functionality of Tutorial Design

This design uses an AND gate with inputs at pins 55 and 63 and output at pin 87. After programming the device, press switches SW1 (pin 55) and SW2 (pin 63) at the same time, and LED DS1 (pin 87) should come ON.

A

Board Connections

This appendix lists the pin assignments and board connections for the ProASIC^{PLUS} Evaluation Board.

Table A-1. Board Connections

Pin Number	APA075	APA150	APA300	APA450	APA600	APA750	APA1000
1	GND	GND	GND	GND	GND	GND	GND
2	I/O	I/O	I/O	I/O	I/O	I/O	I/O
3	I/O	I/O	I/O	I/O	I/O	I/O	I/O
4	I/O	I/O	I/O	I/O	I/O	I/O	I/O
5	I/O	I/O	I/O	I/O	I/O	I/O	I/O
6	I/O	I/O	I/O	I/O	I/O	I/O	I/O
7	I/O	I/O	I/O	I/O	I/O	I/O	I/O
8	I/O	I/O	I/O	I/O	I/O	I/O	I/O
9	I/O	I/O	I/O	I/O	I/O	I/O	I/O
10	I/O	I/O	I/O	I/O	I/O	I/O	I/O
11	I/O	I/O	I/O	I/O	I/O	I/O	I/O
12	I/O	I/O	I/O	I/O	I/O	I/O	I/O
13	I/O	I/O	I/O	I/O	I/O	I/O	I/O
14	I/O	I/O	I/O	I/O	I/O	I/O	I/O
15	I/O	I/O	I/O	I/O	I/O	I/O	I/O
16	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}
17	GND	GND	GND	GND	GND	GND	GND
18	I/O	I/O	I/O	I/O	I/O	I/O	I/O

Table A-1. Board Connections

Pin Number	APA075	APA150	APA300	APA450	APA600	APA750	APA1000
19	I/O	I/O	I/O	I/O	I/O	I/O	I/O
20	I/O	I/O	I/O	I/O	I/O	I/O	I/O
21	I/O	I/O	I/O	I/O	I/O	I/O	I/O
22	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}
23	I/O (GLMX1)	I/O (GLMX1)	I/O (GLMX1)	I/O (GLMX1)	I/O (GLMX1)	I/O (GLMX1)	I/O (GLMX1)
24	GL1	GL1	GL1	GL1	GL1	GL1	GL1
25	AGND	AGND	AGND	AGND	AGND	AGND	AGND
26	NPECL1	NPECL1	NPECL1	NPECL1	NPECL1	NPECL1	NPECL1
27	AVDD	AVDD	AVDD	AVDD	AVDD	AVDD	AVDD
28	PPECL1 (I/P)	PPECL1 (I/P)	PPECL1 (I/P)	PPECL1 (I/P)	PPECL1 (I/P)	PPECL1 (I/P)	PPECL1 (I/P)
29	GND	GND	GND	GND	GND	GND	GND
30	GL2	GL2	GL2	GL2	GL2	GL2	GL2
31	I/O	I/O	I/O	I/O	I/O	I/O	I/O
32	I/O	I/O	I/O	I/O	I/O	I/O	I/O
33	I/O	I/O	I/O	I/O	I/O	I/O	I/O
34	I/O	I/O	I/O	I/O	I/O	I/O	I/O
35	I/O	I/O	I/O	I/O	I/O	I/O	I/O
36	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}
37	I/O	I/O	I/O	I/O	I/O	I/O	I/O
38	I/O	I/O	I/O	I/O	I/O	I/O	I/O

Table A-1. Board Connections

Pin Number	APA075	APA150	APA300	APA450	APA600	APA750	APA1000
39	I/O	I/O	I/O	I/O	I/O	I/O	I/O
40	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}
41	GND	GND	GND	GND	GND	GND	GND
42	I/O	I/O	I/O	I/O	I/O	I/O	I/O
43	I/O	I/O	I/O	I/O	I/O	I/O	I/O
44	I/O	I/O	I/O	I/O	I/O	I/O	I/O
45	I/O	I/O	I/O	I/O	I/O	I/O	I/O
46	I/O	I/O	I/O	I/O	I/O	I/O	I/O
47	I/O	I/O	I/O	I/O	I/O	I/O	I/O
48	I/O	I/O	I/O	I/O	I/O	I/O	I/O
49	I/O	I/O	I/O	I/O	I/O	I/O	I/O
50	I/O	I/O	I/O	I/O	I/O	I/O	I/O
51	I/O	I/O	I/O	I/O	I/O	I/O	I/O
52	GND	GND	GND	GND	GND	GND	GND
53	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}
54	I/O	I/O	I/O	I/O	I/O	I/O	I/O
55	I/O	I/O	I/O	I/O	I/O	I/O	I/O
56	I/O	I/O	I/O	I/O	I/O	I/O	I/O
57	I/O	I/O	I/O	I/O	I/O	I/O	I/O
58	I/O	I/O	I/O	I/O	I/O	I/O	I/O
59	I/O	I/O	I/O	I/O	I/O	I/O	I/O

Table A-1. Board Connections

Pin Number	APA075	APA150	APA300	APA450	APA600	APA750	APA1000
60	I/O	I/O	I/O	I/O	I/O	I/O	I/O
61	I/O	I/O	I/O	I/O	I/O	I/O	I/O
62	I/O	I/O	I/O	I/O	I/O	I/O	I/O
63	I/O	I/O	I/O	I/O	I/O	I/O	I/O
64	I/O	I/O	I/O	I/O	I/O	I/O	I/O
65	GND	GND	GND	GND	GND	GND	GND
66	I/O	I/O	I/O	I/O	I/O	I/O	I/O
67	I/O	I/O	I/O	I/O	I/O	I/O	I/O
68	I/O	I/O	I/O	I/O	I/O	I/O	I/O
69	I/O	I/O	I/O	I/O	I/O	I/O	I/O
70	I/O	I/O	I/O	I/O	I/O	I/O	I/O
71	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}
72	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}
73	I/O	I/O	I/O	I/O	I/O	I/O	I/O
74	I/O	I/O	I/O	I/O	I/O	I/O	I/O
75	I/O	I/O	I/O	I/O	I/O	I/O	I/O
76	I/O	I/O	I/O	I/O	I/O	I/O	I/O
77	I/O	I/O	I/O	I/O	I/O	I/O	I/O
78	I/O	I/O	I/O	I/O	I/O	I/O	I/O
79	I/O	I/O	I/O	I/O	I/O	I/O	I/O
80	I/O	I/O	I/O	I/O	I/O	I/O	I/O

Table A-1. Board Connections

Pin Number	APA075	APA150	APA300	APA450	APA600	APA750	APA1000
81	GND	GND	GND	GND	GND	GND	GND
82	I/O	I/O	I/O	I/O	I/O	I/O	I/O
83	I/O	I/O	I/O	I/O	I/O	I/O	I/O
84	I/O	I/O	I/O	I/O	I/O	I/O	I/O
85	I/O	I/O	I/O	I/O	I/O	I/O	I/O
86	I/O	I/O	I/O	I/O	I/O	I/O	I/O
87	I/O	I/O	I/O	I/O	I/O	I/O	I/O
88	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}
89	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}
90	I/O	I/O	I/O	I/O	I/O	I/O	I/O
91	I/O	I/O	I/O	I/O	I/O	I/O	I/O
92	I/O	I/O	I/O	I/O	I/O	I/O	I/O
93	I/O	I/O	I/O	I/O	I/O	I/O	I/O
94	I/O	I/O	I/O	I/O	I/O	I/O	I/O
95	I/O	I/O	I/O	I/O	I/O	I/O	I/O
96	I/O	I/O	I/O	I/O	I/O	I/O	I/O
97	GND	GND	GND	GND	GND	GND	GND
98	I/O	I/O	I/O	I/O	I/O	I/O	I/O
99	I/O	I/O	I/O	I/O	I/O	I/O	I/O
100	I/O	I/O	I/O	I/O	I/O	I/O	I/O
101	TCK	TCK	TCK	TCK	TCK	TCK	TCK

Table A-1. Board Connections

Pin Number	APA075	APA150	APA300	APA450	APA600	APA750	APA1000
102	TDI	TDI	TDI	TDI	TDI	TDI	TDI
103	TMS	TMS	TMS	TMS	TMS	TMS	TMS
104	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}
105	GND	GND	GND	GND	GND	GND	GND
106	V_{PP}	V_{PP}	V_{PP}	V_{PP}	V_{PP}	V_{PP}	V_{PP}
107	V_{PN}	V_{PN}	V_{PN}	V_{PN}	V_{PN}	V_{PN}	V_{PN}
108	TDO	TDO	TDO	TDO	TDO	TDO	TDO
109	TRST	TRST	TRST	TRST	TRST	TRST	TRST
110	RCK	RCK	RCK	RCK	RCK	RCK	RCK
111	I/O	I/O	I/O	I/O	I/O	I/O	I/O
112	I/O	I/O	I/O	I/O	I/O	I/O	I/O
113	I/O	I/O	I/O	I/O	I/O	I/O	I/O
114	I/O	I/O	I/O	I/O	I/O	I/O	I/O
115	I/O	I/O	I/O	I/O	I/O	I/O	I/O
116	I/O	I/O	I/O	I/O	I/O	I/O	I/O
117	I/O	I/O	I/O	I/O	I/O	I/O	I/O
118	I/O	I/O	I/O	I/O	I/O	I/O	I/O
119	I/O	I/O	I/O	I/O	I/O	I/O	I/O
120	I/O	I/O	I/O	I/O	I/O	I/O	I/O
121	I/O	I/O	I/O	I/O	I/O	I/O	I/O
122	GND	GND	GND	GND	GND	GND	GND

Table A-1. Board Connections

Pin Number	APA075	APA150	APA300	APA450	APA600	APA750	APA1000
123	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}
124	I/O	I/O	I/O	I/O	I/O	I/O	I/O
125	I/O	I/O	I/O	I/O	I/O	I/O	I/O
126	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}
127	I/O	I/O	I/O	I/O	I/O	I/O	I/O
128	GL3	GL3	GL3	GL3	GL3	GL3	GL3
129	PPECL2 (I/P)	PPECL2 (I/P)	PPECL2 (I/P)	PPECL2 (I/P)	PPECL2 (I/P)	PPECL2 (I/P)	PPECL2 (I/P)
130	GND	GND	GND	GND	GND	GND	GND
131	AVDD	AVDD	AVDD	AVDD	AVDD	AVDD	AVDD
132	NPECL2	NPECL2	NPECL2	NPECL2	NPECL2	NPECL2	NPECL2
133	AGND	AGND	AGND	AGND	AGND	AGND	AGND
134	GL4	GL4	GL4	GL4	GL4	GL4	GL4
135	I/O (GLMX2)	I/O (GLMX2)	I/O (GLMX2)	I/O (GLMX2)	I/O (GLMX2)	I/O (GLMX2)	I/O (GLMX2)
136	I/O	I/O	I/O	I/O	I/O	I/O	I/O
137	I/O	I/O	I/O	I/O	I/O	I/O	I/O
138	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}
139	I/O	I/O	I/O	I/O	I/O	I/O	I/O
140	I/O	I/O	I/O	I/O	I/O	I/O	I/O
141	GND	GND	GND	GND	GND	GND	GND
142	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}

Table A-1. Board Connections

Pin Number	APA075	APA150	APA300	APA450	APA600	APA750	APA1000
143	I/O	I/O	I/O	I/O	I/O	I/O	I/O
144	I/O	I/O	I/O	I/O	I/O	I/O	I/O
145	I/O	I/O	I/O	I/O	I/O	I/O	I/O
146	I/O	I/O	I/O	I/O	I/O	I/O	I/O
147	I/O	I/O	I/O	I/O	I/O	I/O	I/O
148	I/O	I/O	I/O	I/O	I/O	I/O	I/O
149	I/O	I/O	I/O	I/O	I/O	I/O	I/O
150	I/O	I/O	I/O	I/O	I/O	I/O	I/O
151	I/O	I/O	I/O	I/O	I/O	I/O	I/O
152	I/O	I/O	I/O	I/O	I/O	I/O	I/O
153	I/O	I/O	I/O	I/O	I/O	I/O	I/O
154	I/O	I/O	I/O	I/O	I/O	I/O	I/O
155	I/O	I/O	I/O	I/O	I/O	I/O	I/O
156	GND	GND	GND	GND	GND	GND	GND
157	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}
158	I/O	I/O	I/O	I/O	I/O	I/O	I/O
159	I/O	I/O	I/O	I/O	I/O	I/O	I/O
160	I/O	I/O	I/O	I/O	I/O	I/O	I/O
161	I/O	I/O	I/O	I/O	I/O	I/O	I/O
162	GND	GND	GND	GND	GND	GND	GND
163	I/O	I/O	I/O	I/O	I/O	I/O	I/O

Table A-1. Board Connections

Pin Number	APA075	APA150	APA300	APA450	APA600	APA750	APA1000
164	I/O	I/O	I/O	I/O	I/O	I/O	I/O
165	I/O	I/O	I/O	I/O	I/O	I/O	I/O
166	I/O	I/O	I/O	I/O	I/O	I/O	I/O
167	I/O	I/O	I/O	I/O	I/O	I/O	I/O
168	I/O	I/O	I/O	I/O	I/O	I/O	I/O
169	I/O	I/O	I/O	I/O	I/O	I/O	I/O
170	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}
171	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}
172	I/O	I/O	I/O	I/O	I/O	I/O	I/O
173	I/O	I/O	I/O	I/O	I/O	I/O	I/O
174	I/O	I/O	I/O	I/O	I/O	I/O	I/O
175	I/O	I/O	I/O	I/O	I/O	I/O	I/O
176	I/O	I/O	I/O	I/O	I/O	I/O	I/O
177	I/O	I/O	I/O	I/O	I/O	I/O	I/O
178	GND	GND	GND	GND	GND	GND	GND
179	I/O	I/O	I/O	I/O	I/O	I/O	I/O
180	I/O	I/O	I/O	I/O	I/O	I/O	I/O
181	I/O	I/O	I/O	I/O	I/O	I/O	I/O
182	I/O	I/O	I/O	I/O	I/O	I/O	I/O
183	I/O	I/O	I/O	I/O	I/O	I/O	I/O
184	I/O	I/O	I/O	I/O	I/O	I/O	I/O

Table A-1. Board Connections

Pin Number	APA075	APA150	APA300	APA450	APA600	APA750	APA1000
185	I/O	I/O	I/O	I/O	I/O	I/O	I/O
186	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}
187	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}
188	I/O	I/O	I/O	I/O	I/O	I/O	I/O
189	I/O	I/O	I/O	I/O	I/O	I/O	I/O
190	I/O	I/O	I/O	I/O	I/O	I/O	I/O
191	I/O	I/O	I/O	I/O	I/O	I/O	I/O
192	I/O	I/O	I/O	I/O	I/O	I/O	I/O
193	I/O	I/O	I/O	I/O	I/O	I/O	I/O
194	I/O	I/O	I/O	I/O	I/O	I/O	I/O
195	GND	GND	GND	GND	GND	GND	GND
196	I/O	I/O	I/O	I/O	I/O	I/O	I/O
197	I/O	I/O	I/O	I/O	I/O	I/O	I/O
198	I/O	I/O	I/O	I/O	I/O	I/O	I/O
199	I/O	I/O	I/O	I/O	I/O	I/O	I/O
200	I/O	I/O	I/O	I/O	I/O	I/O	I/O
201	I/O	I/O	I/O	I/O	I/O	I/O	I/O
202	I/O	I/O	I/O	I/O	I/O	I/O	I/O
203	I/O	I/O	I/O	I/O	I/O	I/O	I/O
204	I/O	I/O	I/O	I/O	I/O	I/O	I/O
205	I/O	I/O	I/O	I/O	I/O	I/O	I/O

Table A-1. Board Connections

Pin Number	APA075	APA150	APA300	APA450	APA600	APA750	APA1000
206	I/O	I/O	I/O	I/O	I/O	I/O	I/O
207	I/O	I/O	I/O	I/O	I/O	I/O	I/O
208	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}

B

Board Schematics

This appendix provides illustrations of the ProASIC^{PLUS} Evaluation Board.

Top-Level View

Figure B-1 illustrates a top-level view of the ProASIC^{PLUS} Evaluation Board.

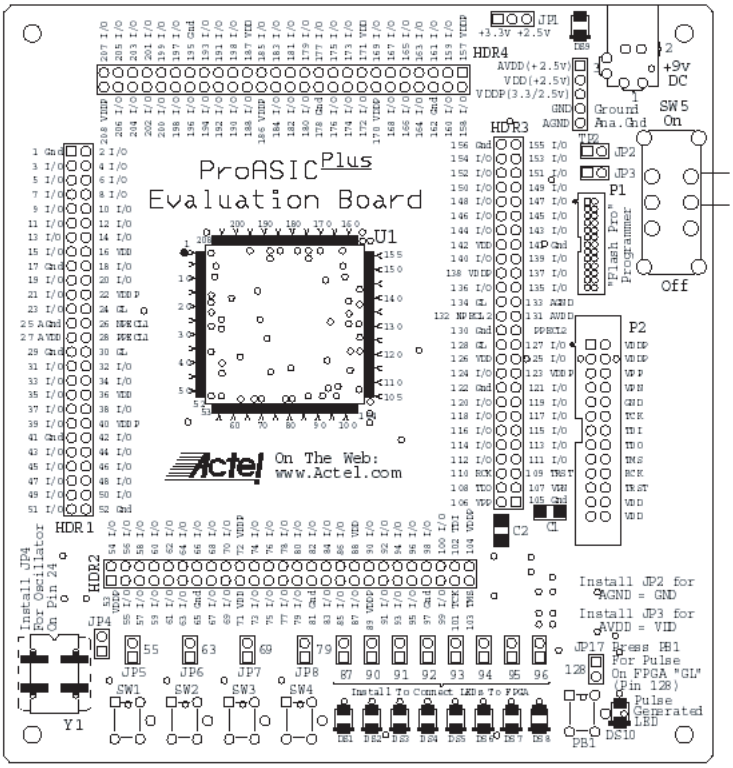


Figure B-1. ProASIC^{PLUS} Evaluation Board: Top-level View

Bottom-Level View

Figure B-2 illustrates a bottom-level view of the ProASIC^{PLUS} Evaluation Board, while Figure B-3 illustrates the ProASIC^{PLUS} Evaluation Board schematic.

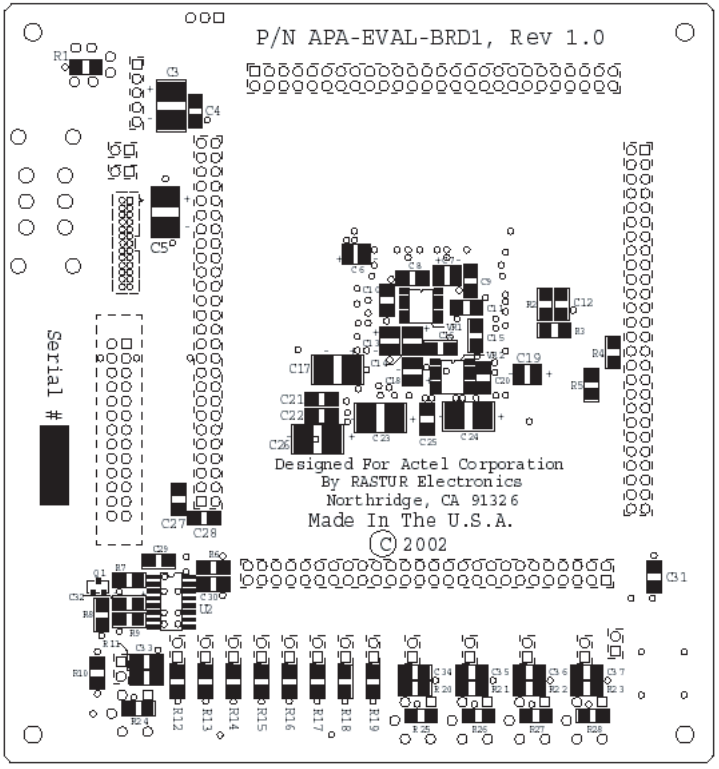


Figure B-2. ProASIC^{PLUS} Evaluation Board: Bottom-level View

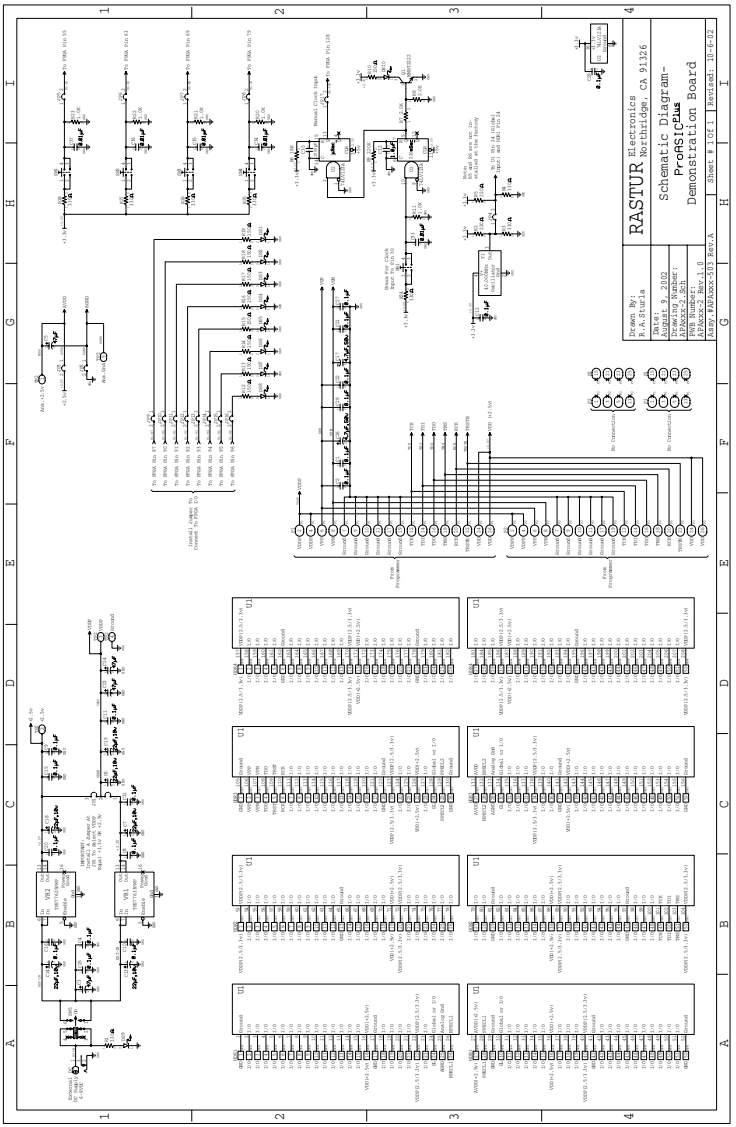


Figure B-3. ProASIC^{PLUS} Evaluation Board Schematic

C

Product Support

Actel backs its products with various support services including Customer Service, a Customer Technical Support Center, a web site, an FTP site, electronic mail, and worldwide sales offices. This appendix contains information about contacting Actel and using these support services.

Actel U.S. Toll-Free Line

Use the Actel toll-free line to contact Actel for sales information, technical support, requests for literature, Customer Service, investor information, and using the Action Facts service.

The Actel toll-free line is (888) 99-ACTEL.

Customer Service

Contact Customer Service for non-technical product support, such as product pricing, product upgrades, update information, order status, and authorization.

Contact Customer Service for non-technical product support, such as product pricing, product upgrades, update information, order status, and authorization.

From Northeast and North Central U.S.A., call **(650) 318-4480**.
From Southeast and Southwest U.S.A., call **(650) 318-4480**.
From South Central U.S.A., call **(650) 318-4434**.
From Northwest U.S.A., call **(650) 318-4434**.
From Canada, call **(650) 318-4480**.
From Europe, call **(650) 318-4252** or +44 (0) 1276 401500.
From Japan, call **(650) 318-4743.**
From the rest of the world, call **(650) 318-4743**.
Fax, from anywhere in the world **(650) 318-8044**.

Actel Customer Technical Support Center

Actel staffs its Customer Technical Support Center with highly skilled engineers who can help answer your hardware, software, and design questions. The Customer Technical Support Center spends a great deal of time creating application notes and

answers to FAQs. So, before you contact us, please visit our online resources. It is very likely we have already answered your questions.

Actel Technical Support

Visit the Actel Customer Support website (http://www.actel.com/custsup/search.html) for more information and support. Many answers available on the searchable web resource include diagrams, illustrations, and links to other resources on the Actel web site.

Web Site

Actel has a World Wide Web home page where you can browse a variety of technical and non-technical information. The URL is http://www.actel.com.

Visit the Actel IP website at http://www.actel.com/ip.

Contacting the Customer Technical Support Center

Highly skilled engineers staff the Technical Support Center from 7:00 A.M. to 6:00 P.M., Pacific Time, Monday through Friday. Several ways of contacting the Center follow:

Electronic Mail

You can communicate your technical questions to our e-mail address and receive answers back by e-mail, fax, or phone. Also, if you have design problems, you can e-mail your design files to receive assistance. We constantly monitor the e-mail account throughout the day. When sending your request to us, please be sure to include your full name, company name, and your contact information for efficient processing of your request.

The technical support e-mail address is **tech@actel.com**.

Telephone

Our Technical Support Center answers all calls. The center retrieves information, such as your name, company name, phone number and your question, and then issues a case number. The Center then forwards the information to a queue where the first available application engineer receives the data and returns your call. The phone

hours are from 7:00 A.M. to 6:00 P.M., Pacific Time, Monday through Friday. The Technical Support numbers are:

(650) 318-4460
(800) 262-1060

Customers needing assistance outside the US time zones can either contact technical support via email (tech@actel.com) or contact a local sales office. Please see our list of Worldwide Sales Offices.

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