

ProASIC^{PLUS} In-System Programming Demonstration Platform



The ProASIC^{PLUS} In-System Programming (ISP) demonstration platform is used to demonstrate the capabilities of Actel's Flash FPGA family (ProASIC^{PLUS}).

The ProASIC^{PLUS} family is intended for high performance, high-density designs with IP cores and customized modules.

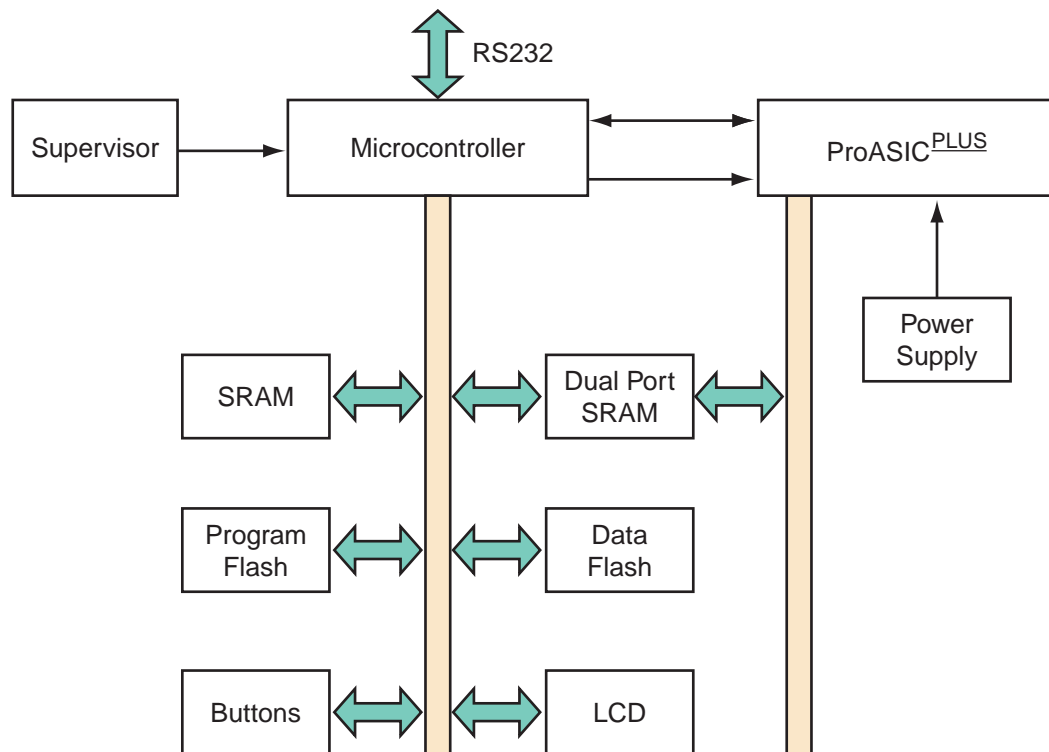


Figure 1 • Block Diagram of the Board

Features

- EZ80 Microcontroller
- LCD display, 2 lines, 16 characters each
- 2 Mbyte SRAM
- UART/DB9 Connector
- 2 Mbyte Flash RAM
- I/O header
- Programming header
- 8 kbyte dual-ported SRAM
- BG456 prototyping socket

Basic Building Blocks

The board contains a Zilog eZ80190 Microprocessor, 2 MB of Flash RAM, and 2 MB of SRAM. An LCD display is available for the user interface with supporting buttons for menu navigation. The dual-ported SRAM can be used to pass messages to and from the ProASIC^{PLUS} and the buttons/LCD. Additionally, a UART/DB9 connector is used to communicate with the PC. Finally, an Actel Flash Pro connector allows programming using an external programmer.

Demonstrating ISP

This board can demonstrate the ISP capability of ProASIC^{PLUS}. The board provides two options for programming the ProASIC^{PLUS} device. A standard Actel JTAG (Flash Pro) header is used for programming with a programmer (Actel's Flash Pro or BP Micro Systems Silicon Sculptor). In addition, the CPU has direct access to the JTAG pins of the FPGA and can control their operation for ISP programming from the Zilog Z80. JTAG programming files in STAPL format are transferred from the PC to this board using the UART. The eZ80 CPU then executes the programming software (STAPL player) pre-stored in the Flash RAM, parses the programming file, and sends out instructions to the JTAG pins of the ProASIC^{PLUS}. For more information on how to implement Internal ISP with Actel's *Performing In-System Programming Using Actel's ProASIC^{PLUS} Devices* application note.

Evaluation/Prototyping

There are two 50 pin 0.1" double-row header sites available on the demo board. These two header sites are connected to unassigned pins of the ProASIC^{PLUS} device, allowing access to a total of 100 I/O pins. These header sites give the user the ability to connect external components to the FPGA or build specific daughter boards that can be connected to the header sites.

Another 35 general purpose I/Os are also connected to a Mictor header for operations that requires high speeds.

Demonstration Application

The demonstration application is an easy-to-use design that allows a ProASIC^{PLUS} APA750 device to write a simple message onto the dual-port SRAM, and in turn, this message is displayed onto the LCD. The ProASIC^{PLUS} demonstration kit does not include an FPGA. Please contact your local Actel representative to order a sample. Before the FPGA is functional, it must be programmed with demonstration designer. This can be done by placing the FPGA into the socket of the demonstration board and programming the FPGA with a Flash Pro or Silicon Sculptor II.

The CD contains all the files (HDL file, Actel ADB file, and STAPL files) needed to run the demonstration application for an APA750. If the designer wants to use the demo design for a ProASIC^{PLUS} device other than that of the APA750, the design must be retargeted to the device using Actel's designer software.; then, a new STAPL file needs to be generated.

Kit Contents

- ProASIC^{PLUS} Demonstration Board
- Power Supply
- RS232 Cable
- CD Contents
 - User Guide
 - Schematic
 - Demo Design Tile
 - PC Host Software

Ordering Information

Ordering Code	Information
APA150-BG456	150,000 Equivalent System Gates FPGA
APA300-BG456	350,000 Equivalent System Gates FPGA
APA450-BG456	450,000 Equivalent System Gates FPGA
APA600-BG456	600,000 Equivalent System Gates FPGA
APA750-BG456	750,000 Equivalent System Gates FPGA
APA1000-BG456	1,000,000 Equivalent System Gates FPGA
Flash Pro	Programmer for Actel's Flash FPGA
Silicon Sculptor II	Production Programmer for all Actel FPGAs

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